TMC22x5y

Multistandard Digital Video Decoder

Three-Line Adaptive Comb Decoder Family, 8 & 10 bit

Features

- Very high performance, low cost
- Adaptive comb-based decoding
- Multiple pin-compatible versions
  - 3-line, 2-line, and band-split
  - 8- and 10-bit processing
- Internal digital linestores
- Supports field- and frame-based decoding
- Multiple input formats
  - CCIR-601/624 (D1), D2, CVBS, YC
- Multiple output formats
  - CCIR-601/624 (D1), RGB, YC_BC_R
- 10-18 Mpps data rate
- Parallel and serial control interface
- Single +5V power supply

Applications

- Studio television equipment
- Personal computer video input
- MPEG and JPEG compression inputs

Description

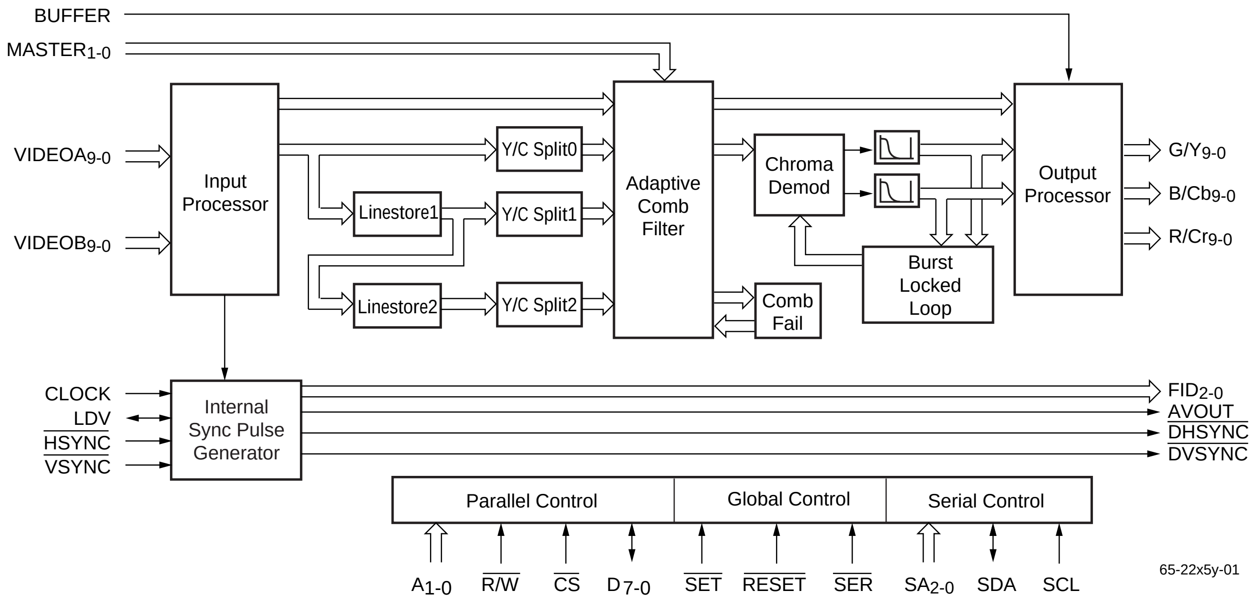
The TMC22x5y family of Digital Video Decoders offers unprecedented, broadcast-quality video processing performance in a single chip. It accepts line-locked or subcarrier-locked composite, YC, or D1 digital video and produces digital components in a variety of formats.

An internal three-line adaptive comb decoder structure produces optimal picture quality with a wide range of source material. Field- and frame-based decoding is supported with external memory. Full comb programmability allows the user to tailor the decoder's response to a particular systems goals.

A family of products offers 3-line, 2-line, and simple decoders in 8-bit and 10-bit versions—all in a pin and software-compatible format. Serial and parallel control ports are provided. These submicron CMOS devices are packaged in a 100-lead Metric Quad Flat Pack (MQFP).

Preliminary Information

Block Diagram



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Preliminary Information

General Description

The TMC22x5y digital decoder can be used as a universal input to digital video processing systems by decoding digital composite video and transcoding digital component inputs into a common data format.

The digital comb filter decoder implements one of sixteen comb filter architectures to produce luminance and color difference component signals which are virtually free of the cross-color and cross-luminance artifacts associated with simple bandsplit filter decoders.

Table 1. TMC22x5y Decoder Family

Function	TMC2215y			TMC2205y		
	3	2	1	3	2	1
10-bit Data	✔	✔	✔			
8-bit Data	✔	✔	✔	✔	✔	✔
D1 Interface	✔	✔	✔	✔	✔	✔
Line-Locked Mode	✔	✔	✔	✔	✔	✔
f_{SC}-Locked Mode	✔	✔	✔	✔	✔	✔
Genlock Mode	✔	✔	✔	✔	✔	✔
Frame-Based Comb	✔			✔		
Field-Based Comb	✔			✔		
3-Line Comb	✔			✔		
2-Line Comb	✔	✔		✔	✔	
Line Grab	✔	✔		✔	✔	
Pixel Grab	✔	✔	✔	✔	✔	✔

Because the cost/performance tradeoff varies among applications, the TMC22x5y decoder has been developed as a family of six parts. They are all assembled in the same package, and fit the same footprint. The register maps are identical.

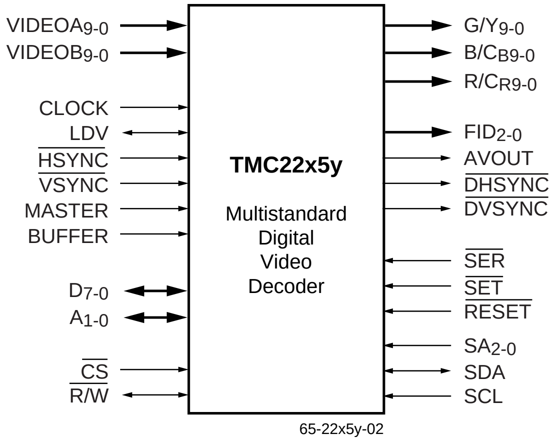


Figure 1. Logic Symbol

The devices come in 8- and 10-bit resolution versions (see Figure 2 for data alignment between 8- and 10-bit versions). Within each resolution version there are three models, offering three-line adaptive comb filtering, two-line adaptive comb filtering, and simple decoding. The TMC22153 10-bit three-line comb filter can be programmed to emulate any of the other parts. All prototyping can be performed with this version to evaluate performance tradeoffs, and lower-cost versions are easily substituted in production.

Input Processor

The digitized video and clocks provided to the decoder can be either locked to the line frequency or the subcarrier frequency of the digitized waveform, providing broadcast quality decoding from the NTSC square pixel rate of 12.27 MHz to the PAL four times subcarrier pixel rate of 17.73 MHz.

MSB					LSB	
VA$_9$ VB$_9$ G/Y$_9$ B/C$_{B9}$ R/C$_{R9}$	VA$_8$ VB$_8$ G/Y$_8$ B/C$_{B8}$ R/C$_{R8}$	•••	VA$_2$ VB$_2$ G/Y$_2$ B/C$_{B2}$ R/C$_{R2}$	VA$_1$ VB$_1$ G/Y$_1$ B/C$_{B1}$ R/C$_{R1}$	VA$_0$ VB$_0$ G/Y$_0$ B/C$_{B0}$ R/C$_{R0}$	10 bit

VA$_9$ VB$_9$ G/Y$_9$ B/C$_{B9}$ R/C$_{R9}$	VA$_8$ VB$_8$ G/Y$_8$ B/C$_{B8}$ R/C$_{R8}$	•••	VA$_2$ VB$_2$ G/Y$_2$ B/C$_{B2}$ R/C$_{R2}$	N/C N/C N/C N/C N/C	N/C N/C N/C N/C N/C	8 bit

Figure 2. Pixel Data Format

Inputs containing embedded GRS (Fairchild Video Input Processors), TRS words (D1 multiplexed component signals), and TRS-ID words (deserialized D2 signals) can be used to lock the internal horizontal and vertical state machines to the embedded information. If this information is not provided, external horizontal and vertical syncs are required for all line-locked input formats, and are optional for NTSC inputs locked to four times the subcarrier (4*Fsc). A simple sync separator is provided for digitized inputs locked to the subcarrier frequency: the internal sync separator locks to the mid point of syncs during the vertical field group, then flywheels during the active portion of the field. For this reason, the $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$ operations are not guaranteed in subcarrier mode.

Adaptive Comb Filter

The line based adaptive comb filter in the TMC22x5y adds or subtracts the high frequency data from three adjacent field lines to produce the average of the high frequency luminance by canceling the chrominance signals, which in flat fields of color are 180 degrees apart. Unfortunately flat fields of color are rare and, when vertical transitions in the picture occur, the output of the comb filter contains a mixture of both high frequency luminance and chrominance, at which time the comb fails. To avoid the comb filter artifacts that occur when this happens, three sets of error signals are sent to a user-programmable lookup table, allowing the output of the comb filter to be mixed with the output of an internal bandsplit decoder.

To produce these comb fail error signals, the video on each of the inputs to the comb filter is passed through a simple bandsplit decoder. The low-frequency portion of the signal is assumed to be luminance and the high frequency portion is processed as chrominance to find the magnitude and phase of the chrominance vector. These three components are then compared across the (0H & 1H) and (1H & 2H) taps of the comb filter to produce the difference in luminance, chrominance magnitude, and chrominance phase. These differences are then translated in the user-programmable lookup table to produce the “K” signal which controls the complementary mix between the output of the comb filter and the simple bandsplit decoder. That is, the “K” signals controls how much of the combed high frequency luminance signal is subtracted from the simple bandsplit chrominance for chroma combs, or added to the low frequency output of the bandsplit for luma comb filters.

Output Processor

The demodulated chrominance signal and the luminance signal are passed through a programmable output matrix, producing RGB, YUV, or YC_BC_R. When the clock is at 27MHz, a D1 signal can be produced on the R/V output with the embedded TRS words fixed to the external $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ timing.

Parallel and Serial Microprocessor Interfaces

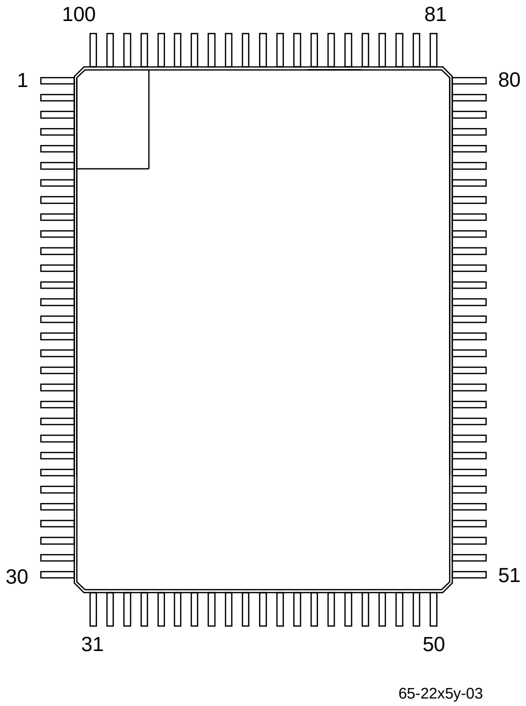
The parallel microprocessor interface employs 12 pins, the serial port uses 5. A single pin, $\overline{\text{SER}}$, selects between the two interface modes.

In parallel interface mode, one address line is decoded for access to the internal control register and its pointer. Controls are reached by loading a desired address through the 8-bit D_{7-0} port, followed by the desired data (read or write) for that address. The control register address pointer auto-increments to address 3Fh and then remains there.

A 2-line serial interface may also be used for initialization and control. The same set of registers accessed by the parallel port is available to the serial port. The device address in the serial interface is selected via pins SA_{2-0}.

The $\overline{\text{RESET}}$ pin sets all internal state machines to their initialized conditions and places the decoder in a power-down mode. All register data are maintained while in power-down mode.

Pin Assignments



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	G/Y_1	26	R/Cr_1	51	$\overline{\text{RESET}}$	76	GND
2	G/Y_0	27	R/Cr_0	52	$\overline{\text{SET}}$	77	VIDEOA_0
3	LDV	28	GND	53	$\overline{\text{SER}}$	78	VIDEOA_1
4	GND	29	V_{DD}	54	SA_0	79	VIDEOA_2
5	V_{DD}	30	AVOUT	55	SA_1	80	VIDEOA_3
6	B/Cb_9	31	FID_0	56	SA_2	81	VIDEOA_4
7	B/Cb_8	32	FID_1	57	GND	82	VIDEOA_5
8	B/Cb_7	33	FID_2	58	SDA	83	VIDEOA_6
9	B/Cb_6	34	$\overline{\text{DHSYNC}}$	59	SCL	84	VIDEOA_7
10	B/Cb_5	35	$\overline{\text{DVSYNC}}$	60	$\overline{\text{CS}}$	85	VIDEOA_8
11	B/Cb_4	36	D_0	61	R/$\overline{\text{W}}$	86	VIDEOA_9
12	B/Cb_3	37	D_1	62	A_0	87	MASTER_0
13	B/Cb_2	38	D_2	63	A_1	88	MASTER_1
14	B/Cb_1	39	GND	64	GND	89	CLOCK
15	B/Cb_0	40	V_{DD}	65	V_{DD}	90	GND
16	GND	41	D_3	66	VIDEOB_0	91	V_{DD}
17	V_{DD}	42	D_4	67	VIDEOB_1	92	GND
18	R/Cr_9	43	D_5	68	VIDEOB_2	93	G/Y_9
19	R/Cr_8	44	D_6	69	VIDEOB_3	94	G/Y_8
20	R/Cr_7	45	D_7	70	VIDEOB_4	95	G/Y_7
21	R/Cr_6	46	GND	71	VIDEOB_5	96	G/Y_6
22	R/Cr_5	47	V_{DD}	72	VIDEOB_6	97	G/Y_5
23	R/Cr_4	48	$\overline{\text{HSYNC}}$	73	VIDEOB_7	98	G/Y_4
24	R/Cr_3	49	$\overline{\text{VSYNC}}$	74	VIDEOB_8	99	G/Y_3
25	R/Cr_2	50	BUFFER	75	VIDEOB_9	100	G/Y_2

Pin Descriptions

Pin Name	Pin Number	Value	Pin Function Description
Inputs			
VIDEOA$_{9-0}$	86, 85, 84, 83, 82, 81, 80, 79, 78, 77	TTL	**Video input A.** An 8 or 10 bit data input to the input multiplexer. For 8-bit versions (TMC2205y) the data are left-justified (VIDEOA$_{9-2}$).
VIDEOB$_{9-0}$	75, 74, 73, 72, 71, 70, 69, 68, 67, 66	TTL	**Video input B.** An 8 or 10 bit data input to the input multiplexer. For 8-bit versions (TMC2205y) the data are left-justified (VIDEOB$_{9-2}$).
$\overline{\text{VSYNC}}$	49	TTL	**Vertical sync input.** A vertical sync signal (active low) occurring at the start of the first vertical sync pulse in a vertical field group. A falling edge of $\overline{\text{VSYNC}}$ which is coincident with a falling edge of $\overline{\text{HSYNC}}$ indicates field 1. This signal is active only when SPGIP$_{1-0}$ = 00.
$\overline{\text{HSYNC}}$	48	TTL	**Horizontal sync input.** A horizontal sync signal (active low) occurring at the falling edge of the video sync. This signal is active only when SPGIP$_{1-0}$ = 00.
MASTER$_{1-0}$	88, 87	TTL	**Master decoder control.** 00 Adaptive comb decoder 01 Simple bandsplit decoder 10 Non adaptive comb filter 11 Flat notched luma and simple bandsplit chroma
BUFFER	50	TTL	**Control register select.** This signal switches between two sets of registers which control the gain or hue values in the output matrix. When BUFFER = 0, registers 17-1F are active. When BUFFER = 1, registers 27-2F take control.
CLOCK	89	TTL	**Master processing clock.** The clock signal can either be at twice the pixel data rate in the line locked modes, or at four times the subcarrier frequency in the subcarrier mode. The interpretation of the CLOCK signal is set by the CKSEL register bit.
$\overline{\text{SET}}$	52	TTL	**Programmable function pin.** The function specified by the SET register is active when $\overline{\text{SET}}$ is low. The decoder returns to its previous operation when $\overline{\text{SET}}$ goes high.
Outputs			
G/Y$_{9-0}$	93, 94, 95, 96, 97, 98, 99, 100, 1, 2	TTL	**Green or Luminance digital output.** For 8-bit versions (TMC2205y) the data are left-justified (G/Y$_{9-2}$).
B/C$_{B9-0}$	6, 7, 8, 9, 10, 11, 12, 13, 14, 15	TTL	**Blue or C$_B$ digital output.** For 8-bit versions (TMC2205y) the data are left-justified (B/C$_{B\ 9-2}$).
R/C$_{R9-0}$	18, 19, 20, 21, 22, 23, 24, 25, 26, 27	TTL	**Red or C$_R$ digital output.** For 8-bit versions (TMC2205y) the data are left-justified (R/C$_{R\ 9-2}$).
$\overline{\text{DVSYNC}}$	35	TTL	**Vertical sync output.** The $\overline{\text{DVSYNC}}$ signal occurs once per field and lasts for 1 video line.
$\overline{\text{DHSYNC}}$	34	TTL	**Horizontal sync output.** The $\overline{\text{DHSYNC}}$ signal occurs once per line and lasts for 64 clock periods.
LDV	3	TTL	**Data synchronization output.** LDV can be an internally or externally generated clock signal. The internal LDV signal is produced when the CLOCK input is at twice the pixel data rate (PXCK); and is a pixel data rate clock phase locked to the falling edge of the HSYNC. The external LDV can be selected under software control, and must be at the CLOCK, or a sub multiple of the CLOCK, frequency.

Pin Descriptions (cont.)

Pin Name	Pin Number	Value	Pin Function Description
AVOUT	30	TTL	**Active video output flag.** The active video output is HIGH during the video portion of each line and LOW during the horizontal and vertical blanking intervals.
FID_{2-0}	33, 32, 31	TTL	**Field identification output.** A 3 bit field ident from the DRS signal.
μP Interface			
D_{7-0}	45, 44, 43, 42, 41, 38, 37, 36	TTL	**Parallel control port data I/O.** All control parameters are loaded into and read back over this 8 bit data port.
A_{1-0}	63, 62	TTL	**Parallel control port address inputs.** These pins govern whether the microprocessor interface selects a table/register address or reads/writes table/register contents.
$\overline{CS}$	60	TTL	**Parallel control port chip select.** When $\overline{CS}$ is high the microprocessor interface port, D_{7-0}, is set to HIGH impedance and ignored. When $\overline{CS}$ is LOW, the microprocessor can read or write parameters over D_{7-0}.
$R/\overline{W}$	61	TTL	**Parallel control port read/write control.** When $R/\overline{W}$ and $\overline{CS}$ are LOW, the microprocessor can write to the control registers or XLUT over D_{7-0}. When $R/\overline{W}$ is HIGH and $\overline{CS}$ is LOW, it can read the contents of any selected XLUT address or control register over D_{7-0}.
$\overline{RESET}$	51	TTL	**Chip master reset.** Bringing $\overline{RESET}$ LOW sets the software reset control bit, $\overline{SRESET}$, LOW and disables the digital outputs. If HRESET is LOW the decoder outputs remain disabled after $\overline{RESET}$ goes HIGH until the $\overline{SRESET}$ bit is set high by the host. If HRESET is HIGH when $\overline{RESET}$ goes HIGH the decoder the internal state machines are enabled.
$\overline{SER}$	53	TTL	**Serial/parallel interface select.** This pin will select between a parallel (HIGH) or serial (LOW) interface port.
SDA	58	R-Bus	**Serial data interface.** Bi-directional serial interface to the control port.
SCL	59	R-Bus	**Serial interface clock.**
SA_{2-0}	56, 55, 54	TTL	**Serial Address.** Three bits providing the lsbs of the serial chip ID used to identify the decoder.
Power Supply			
V_{DD}	5, 17, 29, 40, 47, 65, 91	+5 V	**Power Supply.** Positive power supply for digital circuits, +5V.
GND	4, 16, 28, 39, 46, 57, 64, 76, 90, 92	0.0 V	**Ground.** Ground for digital circuits, 0V.

Control Register Map

The TMC22x5y is initialized and controlled by a set of registers which determine the operating modes.

An external controller is employed to write and read the Control Registers through either the 8-bit parallel or 2-line serial interface port. The parallel port, D_{7-0}, is governed by pins $\overline{\text{CS}}$, $\overline{\text{R/W}}$, and A_{1-0}. The serial port is controlled by SDA and SCL.

Reg	Bit	Name	Function
Global Control			
00	7	SRST	Software reset
00	6	HRST	Hardware reset
00	5-3	SET	$\overline{\text{SET}}$ pin function
00	2	DHVEN	Output H&V sync enable
00	1-0	STD	Selects video standard
Input Processor Control			
01	7		reserved, set to zero
01	6	IPMUX	Input mux control
01	5	IP8B	8 bit input format
01	4	TDEN	TRS detect enable
01	3	TBLK	TRS blank enable
01	2	IPCMSB	Chroma input msb invert
01	1	ABMUX	AB mux control
01	0	CKSEL	Input clock rate select
Burst Loop Control			
02	7		reserved, set to zero
02	6	VIPEN	Video Input Processor enable
02	5-4	LOCK	Global lock mode
02	3	BLM	BLL lock mode
02	2	KILD	Color kill disable
02	1	DMODBY	Demod bypass
02	0	CINT	C_BC_R interpolation enable
Chroma Processor Control			
03	7-5	BLFS	Burst loop filter select
03	4	CCEN	Chroma coring enable
03	3-2	CCOR	Chroma coring threshold
03	1	GAUBY	Gaussian filter bypass
03	0	GAUSEL	Gaussian filter select
Burst Threshold			
04	7-0	BTH	Burst threshold
Pedestal			
05	7-0	PED	Pedestal level
Luma Processor Control			
06	7-6		reserved, set to zero
06	5	ANEN	Adaptive notch enable
06	4	ANR	Adaptive notch rounding
06	3-2	ANT	Adaptive notch threshold
06	1	ANSEL	Adaptive notch select
06	0	NOTCH	Notch enable
Comb Processor Control			
07	7	LS1BY	Line store 1 bypass
07	6	LS1IN	Line store 1 input
07	5	LS2DLY	Line store 2 delay
07	4	SPLIT	Line store 2 data width
07	3	BSFBY	Bandsplit filter bypass
07	2	BSFSEL	Bandsplit filter select
07	1	BSFMSB	Inverts msb of bandsplit filter
07	0	GRSDLY	Delays input to GRS decode by 1H
Mid-Sync Level			
08	7-2	MIDS	Mid-sync level
08	1-0	CLMP	Black level clamp selection
Extended DRS			
09	7-4	PCKF	Clock rate
09	3-0	VSTD	Video standard
Output Control			
0A	7	OP8B	Output rounded to 8 bits
0A	6-5	OPLMT	Output limit select
0A	4-3	MSEN	Mixed sync enable
0A	2	OPCMSB	Chroma output msb invert
0A	1	YBAL	Luma color correction
0A	0	BUREN	Output burst enable
0B	7	FMT422	Enables C_BC_R output mux
0B	6	CDEC	C_BC_R decimation enable
0B	5	YUVT	Enables D1 output
0B	4-2		reserved, set to zero
0B	1	DRSEN	DRS output enable
0B	0	DRSCK	DRS data rate
Comb Filter Control			
0C	7-6	ADAPT	Adaption mode
0C	5	YCES	YC input error signal control
0C	4	YCSEL	luma/chroma comb filter select

Reg	Bit	Name	Function
0C	3-0	COMB	Comb filter architecture
0D	7-6	CEST	Chroma error signal transform
0D	5	CESG	Chroma error signal gain
0D	4	YESG	Luma error signal gain
0D	3	CESTBY	Chroma error signal bypass
0D	2	XFEN	XLUT filter enable
0D	1	FAST	Adaption speed select
0D	0	YWBY	Luma weighting bypass
0E	7-6	XIP	XLUT input select
0E	5-4	XSF	XLUT special function
0E	3-2	YMUX	Y output select
0E	1-0	CMUX	C output select
0F	7		reserved, set to zero
0F	6-5	CAT	Adaption Threshold
0F	4	DCES	D1 C_BC_R error signal
0F	3-2	IPCF	Comb filter input select
0F	1	YCCOMP	YC or Composite input select
0F	0	SYNC	Sync processor select

Sync Pulse Generator

Reg	Bit	Name	Function
10	7-0	STS$_{7-0}$	Sync to sync 8 lsbs
11	7-0	STB	Sync to burst
12	7-0	BTV	Burst to video
13	7-0	AV$_{7-0}$	Active video line 8 lsbs
14	7-6		reserved, set to zero
14	5-4	AV$_{9-8}$	Active video line 2 msbs
14	3		reserved, set to zero
14	2-0	STS$_{10-8}$	Sync to sync 3 msbs
15	7		reserved, set to zero
15	6-2	VINDO	Number of lines in vertical window
15	1	VDIV	Action inside VINDO
15	0	VDOV	Action outside VINDO
16	7-6		reserved, set to zero
16	5-4	NFDLY	new field detect delay
16	3-2	SPGIP	SPG input select
16	1-0	MSIP	Mixed sync separator input select

Buffered register set 0
Active when BUFFER pin set LOW

Reg	Bit	Name	Function
17	7-0	SG0$_{7-0}$	Msync gain, 8 lsbs
18	7-0	YG0$_{7-0}$	Y gain, 8 lsbs
19	7-0	UG0$_{7-0}$	U gain, 8 lsbs
1A	7-0	VG0$_{7-0}$	V gain, 8 lsbs
1B	7-6	YG0$_{9-8}$	Y gain, 2 msbs
1B	5-3	UG0$_{10-8}$	U gain, 3 msbs
1B	2		reserved, set to zero
1B	1-0	VG0$_{9-8}$	V gain, 2 msbs
1C	7-0	YOFF0$_{7-0}$	Y offset, 8 lsbs
1D	7-3		reserved, set to zero
1D	2	YOFF0$_{8}$	Y offset, msb
1D	1-0	SG0$_{7-0}$	Msync gain, 2 msbs
1E	7-0	SYSPH0$_{7-0}$	8 lsbs of phase
1F	7-0	SYSPH0$_{15-8}$	8 msbs of phase

Normalized Subcarrier Frequency

Reg	Bit	Name	Function
20	7-4	FSC$_{3-0}$	Bottom 4 bits of f_{SC}
20	3-0		reserved, set to zero
21	7-0	FSC$_{11-4}$	Lower 8 bits of f_{SC}
22	7-0	FSC$_{19-12}$	Middle 8 bits of f_{SC}
23	7-0	FSC$_{27-20}$	Top 8 bits of f_{SC}
24-25	7-0		reserved, set to zero

Output Format Control

Reg	Bit	Name	Function
26	7-6		reserved, set to zero
26	5	LDVIO	LDV clock select
26	4	OPCKS	Output clock select
26	3	DPCEN	DPC enable
26	2-0	DPC	Decoder product code

Buffered register set 1
Active when BUFFER pin set HIGH

Reg	Bit	Name	Function
27	7-0	SG1$_{7-0}$	Msync gain, 8 lsbs
28	7-0	YG1$_{7-0}$	Y gain, 8 lsbs
29	7-0	UG1$_{7-0}$	U gain, 8 lsbs
2A	7-0	VG1$_{7-0}$	V gain, 8 lsbs
2B	7-6	YG1$_{9-8}$	Y gain, 2 msbs
2B	5-3	UG1$_{10-8}$	U gain, 3 msbs
2B	2		reserved, set to zero
2B	1-0	VG1$_{9-8}$	V gain, 2 msbs
2C	7-0	YOFF1$_{7-0}$	Y offset, 8 lsbs
2D	7-3		reserved, set to zero
2D	2	YOFF1$_{8}$	Y offset, msb
2D	1-0	SG1$_{7-0}$	Msync gain, 2 msbs
2E	7-0	SYSPH1$_{7-0}$	8 lsbs of phase
2F	7-0	SYSPH1$_{15-8}$	8 msbs of phase

Preliminary Information

Reg	Bit	Name	Function
Video Measurement			
30	7		set to zero
30	6	LGF	Line grab flag
30	5	LGEN	Line grab enable
30	4	LGEXT	Ext line grab enable
30	3		reserved, set to zero
30	2	PGG	Pixel grab gate
30	1	PGEN	Pixel grab enable
30	0	PGEXT	Ext pixel grab enable
31	7-0	PG_{7-0}	Pixel grab, 8 lsbs
32	7-0	LG_{7-0}	Line grab, 8 lsbs
33	7		reserved, set to zero
33	6-4	FG	Field grab number
33	3	LG_8	Msb of line grab
33	2-0	PG_{10-8}	Pixel grab, 3 msbs
34	7-0	GY_{9-2}	G/Y grab, 8 msbs
35	7-0	BU_{9-2}	B/U grab, 8 msbs
36	7-0	RV_{9-2}	R/V grab, 8 msbs
37	7-6		reserved
37	5-4	GY_{1-0}	G/Y grab, 2 lsbs
37	3-2	BU_{1-0}	B/U grab, 2 lsbs
37	1-0	RV_{1-0}	R/V grab, 2 lsbs
38	7-0	Y_{9-2}	Luma grab, 8 msbs
39	7-0	M_{9-2}	Msync grab, 8 msbs
3A	7-0	U_{9-2}	U grab, 8 msbs
3B	7-0	V_{9-2}	V grab, 8 msbs
3C	7-6	Y_{1-0}	Luma grab, 2 lsbs
3C	5-4	M_{1-0}	Msync grab, 2 lsbs
3C	3-2	U_{1-0}	U grab, 2 lsbs
3C	1-0	V_{1-0}	V grab, 2 lsbs
Test Control			
3D-3F	7-0	TEST	set to zero
Auto-increment stops at 3F			
Status - Read Only			
40	7-0	DDSPH	DDS phase, 8 msbs
41	7	LINEST	Pixel count reset
41	6	BGST	Start of burst gate
41	5	VACT2	Half line flag
41	4	PALODD	PAL Ident
41	3	VFLY	Vertical count reset
41	2	FGRAB	Field grab
41	1	LGRAB	Line grab
41	0	PGRAB	Pixel grab
42	7	FLD	Field flag (F in D1 output)
42	6	VBLK	Vertical blanking (V in D1 output)
42	5	HBLK	Horizontal blanking (H in D1 output)
42	4-0	LID	Line identification
43	7	YGO	Y/G overflow
43	6	YGU	Y/G underflow
43	5	UBO	C_B/B overflow
43	4	UBU	C_B/B underflow
43	3	VRO	C_R/R overflow
43	2	VRU	C_R/R underflow
43	1-0		reserved
44	7	MONO	Color kill active
44	6-0	FPERR	Frequency/Phase error
45	7-0	DRS	DRS signal
46	7-0	PARTID	Reads back xx_h
47	7-0	REVID	Revision number
48-4A	7-0		reserved
4B	7	PKILL	Phase kill from comb fail
4B	6-5	CFSTAT	Comb filter status
4B	4-0	XOP	XLUT output
4C-FF	7-0		reserved

Notes:

1. Functions are listed in the order of reading and writing.
2. For each register listed above up to register 3F, all bits not specified are reserved and must be set to zero to ensure proper operation.

Control Register Definitions

Global Control Register (00)

7	6	5	4	3	2	1	0
$\overline{\text{SRST}}$	HRST	SET			DHVEN	STD	

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>00</td><td>7</td><td>$\overline{\text{SRST}}$</td><td>Software reset. When LOW, resets and holds internal state machines and disables outputs. When HIGH (normal), starts and runs state machines and enables outputs. This bit is ignored while HRST is high.</td></tr>
<tr><td>00</td><td>6</td><td>HRST</td><td>Hardware reset. When HRST is HIGH, $\overline{\text{SRST}}$ is forced low when $\overline{\text{RESET}}$ pin is taken LOW. State machines are reset and held. When HRST is low the $\overline{\text{RESET}}$ pin can be taken HIGH at any time. The state machines remain disabled until $\overline{\text{SRST}}$ is programmed HIGH. When HRST is high the state machines are enabled as soon as the $\overline{\text{RESET}}$ pin goes HIGH.</td></tr>
<tr><td>00</td><td>5-3</td><td>SET</td><td>$\overline{\text{SET}}$ pin function. These bits control the set function when the $\overline{\text{SET}}$ pin goes low.
A = all outputs high-impedance
B = internal state machines
C = burst locked loop
<table>
<tr><th>SET</th><th>Function</th></tr>
<tr><td>000</td><td>Reset and hold A, B, & C.</td></tr>
<tr><td>001</td><td>Set output to BLUE and flywheel B & C. (RGB outputs)
Set output to "color" and flywheel B & C (YC_BC_R outputs)</td></tr>
<tr><td>010</td><td>Hold A, lock B & C to external input</td></tr>
<tr><td>011</td><td>Reset C only</td></tr>
<tr><td>100</td><td>Reset B & C</td></tr>
<tr><td>101</td><td>Set output to BLUE and lock B & C to input video (RGB output)</td></tr>
<tr><td>110</td><td>Line and pixel grab depending on $VMCR_{6-0}$ (reg 30)</td></tr>
<tr><td>111</td><td>Toggle reset function of SET = 010. For each $\overline{\text{SET}}$ = 0 pulse the chip operation will change from normal to that of SET = 010 or visa versa.</td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td>The first $\overline{\text{SET}}$ pulse after a software or hardware reset, with SET = 111, causes a toggle to SET = 010.</td></tr>
<tr><td>00</td><td>2</td><td>DHVEN</td><td>Output H&V sync enable. Disables $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$ signals when HIGH.</td></tr>
<tr><td>00</td><td>1-0</td><td>STD</td><td>Selects video standard. Selects video standard.
<table>
<tr><th>SET</th><th>Function</th></tr>
<tr><td>00</td><td>NTSC</td></tr>
<tr><td>01</td><td>reserved</td></tr>
<tr><td>10</td><td>PAL/M</td></tr>
<tr><td>11</td><td>All PAL standards except PAL/M</td></tr>
</table></td></tr>
</table>

Control Register Definitions (continued)

Input Processor Control (01)

7	6	5	4	3	2	1	0
Reserved	IPMUX	IP8B	TDEN	TBLK	IPCMSB	ABMUX	CKSEL

Reg	Bit	Name	Description
01	7	Reserved	**Reserved, set to zero.**
01	6	IPMUX	**Input mux control.** Used to select the Video Input Processor, D1, or D2 data as the VA input to the input processor. VIDEOA is selected for VA and VIDEOB is selected for VB when IPMUX is set LOW. VIDEOB is selected for VA and VIDEOA for VB when IPMUX is set HIGH. For YC inputs, the luma data must be passed through the VA input and chroma through the VB input. IPMUX should be set LOW for line locked composite inputs.
01	5	IP8B	**8 bit input format.** Bottom two bits of inputs VIDEOA$_{9-0}$ and VIDEOB$_{9-0}$ are set to zero when HIGH.
01	4	TDEN	**TRS detect enable.** When HIGH, the TRS words embedded in incoming video are used to reset the horizontal and vertical state machines. When LOW the externally provided or internally generated HSYNC and VSYNC are used to reset the horizontal and vertical state machines.
01	3	TBLK	**TRS blank enable.** Blanks the TRS and AUX data words when HIGH. For line locked and D1 data, the TRS and AUX data words are set to the luma and chroma blanking levels as appropriate. For D2 (4*f$_{SC}$) data, the TRS and AUX data words are set to the sync tip level.
01	2	IPCMSB	**Chroma input msb invert.** The msb of the chroma or C$_B$C$_R$ data are inverted when HIGH.
01	1	ABMUX	**AB mux control.** Selects the primary and secondary inputs to the decoder from the DA and DB outputs of the input processor. When ABMUX is LOW, DA is selected as the primary and DB as the secondary decoder input.
01	0	CKSEL	**Input clock rate select.** Set HIGH for line locked clocks and LOW for subcarrier locked clocks. Line locked clocks should be at twice the pixel data rate, and the subcarrier clock should be at four times the subcarrier frequency.

Control Register Definitions (continued)

Burst Loop Control (02)

7	6	5	4	3	2	1	0
Reserved	VIPEN	LOCK		BLM	KILD	DMODBY	CINT

Reg	Bit	Name	Description
02	7	Reserved	**Reserved, set to zero.**
02	6	VIPEN	**Video Input Processor enable.** Selects interface protocol for Fairchild video input devices. Active only when LOCK$_{1-0}$ = 10. **VIPEN** / **Function** 0 / Video Input Processor Interface 1 / TMC22071 Interface
02	5-4	LOCK	**Global Lock mode.** Sets the decoder locking mode. **LOCK** / **Function** 00 / Line Locked Mode 01 / Subcarrier Locked Mode 10 / Video Input Processor Mode 11 / D1 Mode
02	3	BLM	**BLL lock mode.** Sets the decoder burst locking mode. **BLM** / **Function** 0 / Frequency Lock 1 / Phase Lock
02	2	KILD	**Color kill disable.** Color killer is disabled when HIGH.
02	1	DMODBY	**Demod bypass.** Chroma data bypasses the demodulator when HIGH.
02	0	CINT	**C_BC_R interpolation enable.** Interpolation of C_BC_R input data from 0:2:2 to 0:4:4 is enabled when HIGH.

Control Register Definitions (continued)

Chroma Processor Control (03)

7	6	5	4	3	2	1	0
BLFS			CCEN	CCOR		GAUBY	GAUSEL

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>03</td><td>7-5</td><td>BLFS</td><td>Burst loop filter select.
<table>
<tr><th>BLFS</th><th>fS (Mpps)</th><th>Recommended Criteria</th></tr>
<tr><td>000</td><td>13.5</td><td>PAL, Line-Locked YC</td></tr>
<tr><td>000</td><td>15</td><td>PAL, Line-Locked YC</td></tr>
<tr><td>001</td><td>12.27</td><td>NTSC, Line-Locked YC</td></tr>
<tr><td>001</td><td>13.5</td><td>PAL, Line-Locked Composite</td></tr>
<tr><td>010</td><td>13.5</td><td>NTSC, Line-Locked YC</td></tr>
<tr><td>010</td><td>15</td><td>PAL, Line-Locked Composite</td></tr>
<tr><td>011</td><td>14.32</td><td>NTSC, Subcarrier-Locked YC</td></tr>
<tr><td>011</td><td>17.73</td><td>PAL, Subcarrier-Locked Composite</td></tr>
<tr><td>100</td><td>17.73</td><td>PAL, Subcarrier-Locked YC</td></tr>
<tr><td>101</td><td>13.5</td><td>NTSC, Line-Locked Composite</td></tr>
<tr><td>110</td><td>12.27</td><td>NTSC, Line-Locked Composite</td></tr>
<tr><td>111</td><td>14.32</td><td>NTSC, Subcarrier-Locked Composite</td></tr>
</table></td></tr>
<tr><td>03</td><td>4</td><td>CCEN</td><td>Chroma coring enable. Enables Chroma Coring when HIGH.</td></tr>
<tr><td>03</td><td>3-2</td><td>CCOR</td><td>Chroma coring threshold. Sets the Chroma Coring threshold.
<table>
<tr><th>CCOR</th><th>Function</th></tr>
<tr><td>00</td><td>1 lsb</td></tr>
<tr><td>01</td><td>2 lsb</td></tr>
<tr><td>10</td><td>3 lsb</td></tr>
<tr><td>11</td><td>4 lsb</td></tr>
</table></td></tr>
<tr><td>03</td><td>1</td><td>GAUBY</td><td>Gaussian filter bypass. The chroma data bypasses the Gaussian LPF when HIGH.</td></tr>
<tr><td>03</td><td>0</td><td>GAUSEL</td><td>Gaussian LPF select. Selects the Gaussian filter response to be used on the demodulated chrominance.
<table>
<tr><th>GAUSEL</th><th>Function</th></tr>
<tr><td>0</td><td>Select Gaussian LPF resp. 2</td></tr>
<tr><td>1</td><td>Select Gaussian LPF resp. 1</td></tr>
</table>
See Figure 6 for filter responses.</td></tr>
</table>

Control Register Definitions (continued)

Burst Threshold (04)

7	6	5	4	3	2	1	0
BTH							

Reg	Bit	Name	Description
04	7-0	BTH	**Burst threshold.** The 8 bit value to be compared against the demodulated U and V component data. If over 127 lines occur in a field in which the burst is below this threshold, then the color is set to chroma black for the next field.

Pedestal (05)

7	6	5	4	3	2	1	0
PED							

Reg	Bit	Name	Description
05	7-0	PED	**Pedestal level.** An 8 bit magnitude subtracted from the luma data to remove the setup before processing by the output matrix.

Luma Processor Control (06)

7	6	5	4	3	2	1	0
Reserved		ANEN	ANR	ANT		YSEL	NOTCH

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>06</td><td>7-6</td><td>Reserved</td><td>Reserved, set to zero.</td></tr>
<tr><td>06</td><td>5</td><td>ANEN</td><td>Adaptive notch enable. Enables adaptive notch when HIGH.</td></tr>
<tr><td>06</td><td>4</td><td>ANR</td><td>Adaptive notch rounding. Sets adaptive notch rounding point.
<table>
<tr><th>ANR</th><th>Function</th></tr>
<tr><td>0</td><td>Round to 10 bits</td></tr>
<tr><td>1</td><td>Round to 8 bits</td></tr>
</table></td></tr>
<tr><td>06</td><td>3-2</td><td>ANT</td><td>Adaptive notch threshold level. Sets the adaptive notch threshold.
<table>
<tr><th>ANT</th><th>Function</th></tr>
<tr><td>00</td><td>Magnitude difference less than 32</td></tr>
<tr><td>01</td><td>Magnitude difference less than 24</td></tr>
<tr><td>10</td><td>Magnitude difference less than 16</td></tr>
<tr><td>11</td><td>Magnitude difference less than 8</td></tr>
</table></td></tr>
<tr><td>06</td><td>1</td><td>YSEL</td><td>Adaptive notch select. Selects adaptive notch filter response.
<table>
<tr><th>YSEL</th><th>Function</th></tr>
<tr><td>0</td><td>Adaptive notch response ANF1</td></tr>
<tr><td>1</td><td>Adaptive notch response ANF2</td></tr>
</table></td></tr>
<tr><td>06</td><td>0</td><td>NOTCH</td><td>Notch enable. Adaptive notch filter ANF3 selected when HIGH and ANEN is HIGH, non-adaptive notch filter selected when HIGH and ANEN is LOW. Function may be overridden by XSF (Reg 0E, bits 5-4).</td></tr>
</table>

Preliminary Information

Control Register Definitions (continued)

Comb Processor Control (07)

7	6	5	4	3	2	1	0
LS1BY	LS1IN	LS2DLY	SPLIT	BSFBY	BSFSEL	BSFMSB	GRSDLY

Reg	Bit	Name	Description
07	7	LS1BY	**Line store 1 bypass.** Bypasses linestore 1 when HIGH.
07	6	LS1IN	**Line store 1 input.** Selects the input of linestore 1:
07	5	LS2DLY	**Line store 2 delay.** LSTORE2 uses STS to store 1H when LOW and uses VL to store SAV to EAV (or max count) when HIGH.
07	4	SPLIT	**Line store 2 delay.** Splits data through LSTORE2, 9 bits chroma and 7 bits luma when HIGH (chroma combs) and 8 bits chroma and 8 bits luma when LOW (luma comb).
07	3	BSFBY	**Bandsplit filter bypass.** Bandsplit filter is bypassed when HIGH.
07	2	BSFSEL	**Bandsplit filter select.** Selects the bandsplit filter to be used:
07	1	BSFMSB	**Inverts msb of bandsplit filter.** When HIGH, inverts the msb of the input to the bandsplit filter.
07	0	GRSDLY	**Delays input to GRS decode.** When HIGH, delays the input to the GRS extraction circuit by 1H.

LS1IN	Function
0	Primary Input
1	Secondary Input

BSFSEL	Function
0	Select bandsplit filter response 1
1	Select bandsplit filter response 2

Mid-Sync Level (08)

7	6	5	4	3	2	1	0
MIDS							

Reg	Bit	Name	Description
08	7-2	MIDS	**Mid sync level.** Sets the mid point of syncs in the mixed sync separator, in the subcarrier locked mode.
08	1-0	CLMP	**Clamp input selection**

CLMP[1:0]	Function
00	Clamp disabled, black level set to 240
01	Clamp disabled, black level set to 256
10	Clamp enabled, use VIDEOB as reference
11	Clamp enabled, use internal LPF as reference

Notes: 1. CLMP[1:0] controls the clamp algorithm in silicon revision G only. For silicon revisions A through F these two bits provide the lsbs of the sync level selection.

Control Register Definitions (continued)

Extended DRS (09)

7	6	5	4	3	2	1	0
PCKF				VSTD			

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>09</td><td>7-4</td><td>PCKF</td><td>Clock rate.
<table>
<tr><th>PCKF</th><th>Function</th></tr>
<tr><td>0000</td><td>13.50 MHz</td></tr>
<tr><td>0001</td><td>reserved</td></tr>
<tr><td>0010</td><td>reserved</td></tr>
<tr><td>0011</td><td>reserved</td></tr>
<tr><td>0100</td><td>14.32 MHz</td></tr>
<tr><td>0101</td><td>17.73 MHz</td></tr>
<tr><td>0110</td><td>reserved</td></tr>
<tr><td>0111</td><td>reserved</td></tr>
<tr><td>1000</td><td>12.27 MHz</td></tr>
<tr><td>1001</td><td>14.75 MHz</td></tr>
<tr><td>1010</td><td>15.00 MHz</td></tr>
<tr><td>1011</td><td>reserved</td></tr>
<tr><td>1100</td><td>reserved</td></tr>
<tr><td>1101</td><td>reserved</td></tr>
<tr><td>1110</td><td>reserved</td></tr>
<tr><td>1111</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>09</td><td>3-0</td><td>VSTD</td><td>Video Standard. Selects the video standard.
<table>
<tr><th>VSTD</th><th>Function</th></tr>
<tr><td>0000</td><td>NTSC-M</td></tr>
<tr><td>0001</td><td>NTSC-EIAJ</td></tr>
<tr><td>0010</td><td>reserved</td></tr>
<tr><td>0011</td><td>reserved</td></tr>
<tr><td>0100</td><td>reserved</td></tr>
<tr><td>0101</td><td>reserved</td></tr>
<tr><td>0110</td><td>reserved</td></tr>
<tr><td>0111</td><td>reserved</td></tr>
<tr><td>1000</td><td>PAL-B, G, H, I</td></tr>
<tr><td>1001</td><td>PAL-M</td></tr>
<tr><td>1010</td><td>PAL-N (Argentina, Paraguay, Uruguay)</td></tr>
<tr><td>1011</td><td>PAL-N (Jamaica)</td></tr>
<tr><td>1100</td><td>reserved</td></tr>
<tr><td>1101</td><td>reserved</td></tr>
<tr><td>1110</td><td>reserved</td></tr>
<tr><td>1111</td><td>reserved</td></tr>
</table></td></tr>
</table>

Control Register Definitions (continued)

Output Control (0A)

7	6	5	4	3	2	1	0
OP8B	OPLMT	OPLMT	MSEN		OPCMSB	YBAL	BUREN

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0A</td><td>7</td><td>OP8B</td><td>Output rounded to 8 bits. Rounds the outputs to 8 bits when HIGH. The two lsbs are set to zero.</td></tr>
<tr><td>0A</td><td>6-5</td><td>OPLMT</td><td>Output limit select. Sets the output format and limiters:
<table>
<tr><th>OPLMT</th><th>Function</th></tr>
<tr><td>00</td><td>RGB output format
Limited to 0 to 1023</td></tr>
<tr><td>01</td><td>YCBCR output format
Y limited to 0 to 1023
CBCR limited to ±511</td></tr>
<tr><td>10</td><td>RGB output format
Limited to 64 to 940</td></tr>
<tr><td>11</td><td>YCBCR output format
Y limited to 64 to 940
CBCR limited to ±448</td></tr>
</table></td></tr>
<tr><td>0A</td><td>4-3</td><td>MSEN</td><td>Mixed sync enable. Sets composite sync output format:
<table>
<tr><th>MSEN</th><th>Function</th></tr>
<tr><td>00</td><td>No sync, & “super blacks” disabled</td></tr>
<tr><td>01</td><td>No sync, & “super blacks” disabled</td></tr>
<tr><td>10</td><td>Sync on G/Y output only, & “super blacks” enabled</td></tr>
<tr><td>11</td><td>Sync on RGB outputs, & “super blacks” enabled</td></tr>
</table></td></tr>
<tr><td>0A</td><td>2</td><td>OPCMSB</td><td>Chroma output msb invert. Inverts the msb of the CBCR or Chroma output when HIGH.</td></tr>
<tr><td>0A</td><td>1</td><td>YBAL</td><td>Luma color correction. Setting this bit HIGH forces the chroma to zero whenever the luma equals or exceeds the luma limit.</td></tr>
<tr><td>0A</td><td>0</td><td>BUREN</td><td>Output burst enable. When HIGH, passes the burst through on the chroma channel. Sets the burst region to zero when LOW.</td></tr>
</table>

Notes: 1. To enable “super blacks” and disable syncs of the output simply set MSEN[1] HIGH and the sync gain to zero.

Control Register Definitions (continued)

Output Control (0B)

7	6	5	4	3	2	1	0
FMT422	CDEC	YUVT	Reserved			DRSEN	DRSCK

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0B</td><td>7</td><td>FMT422</td><td>Enables C_BC_R output mux. When HIGH, multiplexes the C_B and C_R data onto the same data bus. The chroma or multiplexed C_BC_R output appears on the B/C_B output. The R/C_R output is forced low.</td></tr>
<tr><td>0B</td><td>6</td><td>CDEC</td><td>C_BC_R decimation enable. When HIGH, the C_BC_R data are decimated to 0:2:2 in the output processor.</td></tr>
<tr><td>0B</td><td>5</td><td>YUVT</td><td>Enables D1 output. When HIGH, enables 4:2:2 multiplexed YC_BC_R onto the R/C_R data output with TRS words inserted into the output data stream. The Y data are still available on the G/Y output and multiplexed C_BC_R is available on the B/U output.</td></tr>
<tr><td>0B</td><td>4-2</td><td>Reserved</td><td>Reserved, set to zero.</td></tr>
<tr><td>0B</td><td>1</td><td>DRSEN</td><td>DRS output enable. When HIGH, enables the DRS onto the G/Y output.</td></tr>
<tr><td>0B</td><td>0</td><td>DRSCK</td><td>DRS data rate. Sets the DRS output data rate.
<table>
<tr><th>DRSCK</th><th>Function</th></tr>
<tr><td>0</td><td>Embeds data bytes (8 bits) at PCK clock rate</td></tr>
<tr><td>1</td><td>Embeds data nibbles (4 bits) at PXCK clock rate</td></tr>
</table></td></tr>
</table>

Control Register Definitions (continued)

Comb Filter Control (0C)

7	6	5	4	3	2	1	0
ADAPT		YCES	YCSEL	COMB			

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0C</td><td>7-6</td><td>ADAPT</td><td>Adaption mode. Sets the 3-line comb filter adaption mode in NTSC.
<table>
<tr><th>ADAPT[1:0]</th><th>Function</th></tr>
<tr><td>00</td><td>Adapts to best of 3 types of line based comb filters in NTSC only.</td></tr>
<tr><td>01</td><td>Adapts to the best of two field or frame based comb in NTSC only.</td></tr>
<tr><td>10</td><td>3 line (tap) comb only. Never adapts to a 2 line (tap) filter. The higher set of comb filter error signals are sent to the XLUT. NTSC or PAL comb filter.</td></tr>
<tr><td>11</td><td>Adapts to best of two 3 line chroma comb filters in PAL only.</td></tr>
</table></td></tr>
<tr><td>0C</td><td>5</td><td>YCES</td><td>YC input error signal control. Error signal control for YC input, luma comb.
<table>
<tr><th>YCES</th><th>Function</th></tr>
<tr><td>0</td><td>LPF and HPF error signal, between (0H & 1H) or (1H & 2H) in NTSC or between (0H & 2H) in PAL,are sent to XLUT</td></tr>
<tr><td>1</td><td>LPF error signal, between (0H & 1H) and (1H & 2H) in NTSC or between (0H & 2H) in PAL, are sent to XLUT</td></tr>
</table></td></tr>
<tr><td>0C</td><td>4</td><td>YCSEL</td><td>Luma/chroma comb filter select. Selects luma or chroma comb filter.
<table>
<tr><th>YCSEL</th><th>Function</th></tr>
<tr><td>0</td><td>Chroma comb filter</td></tr>
<tr><td>1</td><td>Luma comb filter</td></tr>
</table></td></tr>
<tr><td>0C</td><td>3-0</td><td>COMB</td><td>Comb filter architecture.
<table>
<tr><th>COMB</th><th>Function</th></tr>
<tr><td colspan="2"><i>YC or composite comb filter architectures</i></td></tr>
<tr><td>0000</td><td>PAL or NTSC 3 line comb</td></tr>
<tr><td>0001</td><td>NTSC 3 line comb (0H & 1H)</td></tr>
<tr><td>0010</td><td>NTSC 3 line comb (1H & 2H)</td></tr>
<tr><td>0011</td><td>NTSC 2 line comb (0H & 1H)</td></tr>
<tr><td>0100</td><td>NTSC (2 line) field comb</td></tr>
<tr><td>0101</td><td>NTSC or PAL field comb</td></tr>
<tr><td>0110</td><td>NTSC (2 line) frame comb</td></tr>
<tr><td>0111</td><td>NTSC or PAL frame comb</td></tr>
<tr><td colspan="2"><i>D1 comb filter architectures</i></td></tr>
<tr><td>1000</td><td>3 line comb</td></tr>
<tr><td>1001</td><td>3 line comb (0H & 1H)</td></tr>
<tr><td>1010</td><td>3 line comb (1H & 2H)</td></tr>
<tr><td>1011</td><td>3 line comb (0H & 2H)</td></tr>
<tr><td>1100</td><td>(2 line) field comb</td></tr>
<tr><td>1101</td><td>field or 2 line (0H & 1H) comb</td></tr>
<tr><td>1110</td><td>(2 line) frame comb</td></tr>
<tr><td>1111</td><td>frame comb</td></tr>
</table></td></tr>
</table>

Control Register Definitions (continued)

Comb Filter Control (0D)

7	6	5	4	3	2	1	0
CEST		CESG	YESG	CESTBY	XFEN	FAST	YWBY

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0D</td><td>7-6</td><td>CEST</td><td>Chroma error signal transform.
<table>
<tr><th>CEST</th><th>Video Standard</th><th>Clock Rate (MHz)</th></tr>
<tr><td>00</td><td>PAL/NTSC</td><td>4*Fsc & 13.5MHz</td></tr>
<tr><td>01</td><td>NTSC</td><td>12.27MHz</td></tr>
<tr><td>10</td><td>PAL</td><td>14.75MHz</td></tr>
<tr><td>11</td><td>PAL</td><td>15MHz</td></tr>
</table></td></tr>
<tr><td>0D</td><td>5</td><td>CESG</td><td>Chroma error signal gain.
<table>
<tr><th>CESG</th><th>Function</th></tr>
<tr><td>0</td><td>Normal chroma fail signal levels</td></tr>
<tr><td>1</td><td>Double the chroma error signal levels</td></tr>
</table></td></tr>
<tr><td>0D</td><td>4</td><td>YESG</td><td>Luma error signal gain.
<table>
<tr><th>YESG</th><th>Function</th></tr>
<tr><td>0</td><td>Normal luma fail signal levels</td></tr>
<tr><td>1</td><td>Double the luma error signal levels</td></tr>
</table></td></tr>
<tr><td>0D</td><td>3</td><td>CESTBY</td><td>Chroma error signal bypass. When HIGH, bypasses chroma error signal.</td></tr>
<tr><td>0D</td><td>2</td><td>XFEN</td><td>XLUT filter enable. When HIGH, enables the LPF on the XLUT output.</td></tr>
<tr><td>0D</td><td>1</td><td>FAST</td><td>Adaption speed select. When HIGH, the 3 line comb filter selects between comb filter architectures on a pixel by pixel basis. When LOW, the selection is filtered.</td></tr>
<tr><td>0D</td><td>0</td><td>YWBY</td><td>Luma weighting bypass. When HIGH bypasses the luma fail weighting.</td></tr>
</table>

Control Register Definitions (continued)

Comb Filter Control (0E)

7	6	5	4	3	2	1	0
XIP		XSF		YMUX		CMUX	

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0E</td><td>7-6</td><td>XIP</td><td>XLUT input select. Selects the comb fail signals presented to the XLUT:
<table>
<tr><th>XIP[1:0]</th><th>Input to XLUT</th></tr>
<tr><td>00</td><td>2 bits of phase error (X[7:6]), 3 bits of chroma (X[5:3]) and luma magnitude error (X[3:0]).</td></tr>
<tr><td>01</td><td>4 bits of chroma (X[7:4]) and luma magnitude error (X[3:0]).</td></tr>
<tr><td>10</td><td>3 bits of phase error (X[7:5]), 3 bits of chroma magnitude error (X[4:2]), and 2 bits of luma magnitude error (X[1:0]).</td></tr>
<tr><td>11</td><td>4 bits of phase error (X[7:4]) and chroma magnitude error (X[3:0]).</td></tr>
</table></td></tr>
<tr><td>0E</td><td>5-4</td><td>XSF</td><td>XLUT special function.
<table>
<tr><th>XSF</th><th>Luma</th><th>Chroma</th></tr>
<tr><td>00</td><td>Comb</td><td>Simple</td></tr>
<tr><td>01</td><td>Simple</td><td>Comb</td></tr>
<tr><td>10</td><td>Flat with notch</td><td>Simple</td></tr>
<tr><td>11</td><td>Flat with notch</td><td>Comb</td></tr>
</table></td></tr>
<tr><td>0E</td><td>3-2</td><td>YMUX</td><td>Y output select. Output selection of luma 4:1 mux
<table>
<tr><th>YMUX</th><th>Output</th></tr>
<tr><td>00</td><td>Comb</td></tr>
<tr><td>01</td><td>Flat - Comb</td></tr>
<tr><td>10</td><td>Flat</td></tr>
<tr><td>11</td><td>Simple</td></tr>
</table></td></tr>
<tr><td>0E</td><td>1-0</td><td>CMUX</td><td>C output select. Output selection of chroma 4:1 mux
<table>
<tr><th>CMUX</th><th>Output</th></tr>
<tr><td>00</td><td>Comb</td></tr>
<tr><td>01</td><td>Flat - Comb</td></tr>
<tr><td>10</td><td>Flat</td></tr>
<tr><td>11</td><td>Simple</td></tr>
</table></td></tr>
</table>

Control Register Definitions (continued)

Comb Filter Control (0F)

7	6	5	4	3	2	1	0
Reserved	CAT		DCES	IPCF		YCCOMP	SYNC

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0F</td><td>7</td><td>Reserved</td><td>Reserved, set to zero.</td></tr>
<tr><td>0F</td><td>6-5</td><td>CAT</td><td>Adaption threshold. Fixes threshold at which different comb filters are selected.
<table>
<tr><td>0</td><td>0</td><td>5% of max error</td></tr>
<tr><td>0</td><td>1</td><td>15% of max error</td></tr>
<tr><td>1</td><td>0</td><td>25% of max error</td></tr>
<tr><td>1</td><td>1</td><td>50% of max error</td></tr>
</table></td></tr>
<tr><td>0F</td><td>4</td><td>DCES</td><td>D1 C_BC_R error signal. When set LOW for D1 chroma comb filters:
a) In 3 line comb filter architectures, the magnitude error between the component data for that pixel selects the 3 line comb or adapts to a 2 line comb. On a “C_B pixel” the error signal selected on pixel (x+4) is sent to the XLUT with the magnitude difference between “C_R pixels” on the same piar of lines, but from pixel (x+3). Likewise on a “C_R pixel” the error signal selected on pixel (x+5) is sent to the XLUT with the magnitude difference between “C_B pixels” on the same lines but from pixel (x+4).
b) In 2 line comb filters the magnitude differences between the same pair of lines is always sent to the XLUT, On a “C_B pixel” the error from the preceding “C_R pixel” is used and on a “C_R pixel” the preceding “C_B pixel” would be used.
When set HIGH for D1 chroma filters:
This is used for 3 line comb filter architecture that are inhibited from adapting to 2 line comb filter architectures. The input to the XLUT is the magnitude error in C_R between (0H & 1H) and (1H & 2H) on “C_R pixels” and the magnitude error between (0H & 1H) and (1H & 2H) on “C_B pixels”.</td></tr>
<tr><td>0F</td><td>3-2</td><td>IPCF</td><td>Comb filter input select. Selects primary inputs to the comb filter.
<table>
<tr><th>IPCF</th><th>Function</th></tr>
<tr><td>0 0</td><td>Flat video</td></tr>
<tr><td>0 1</td><td>LPF output</td></tr>
<tr><td>1 0</td><td>HPF output</td></tr>
<tr><td>1 1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>0F</td><td>1</td><td>YCCOMP</td><td>YC or Composite input select. Selects YC inputs when HIGH and composite inputs when LOW.</td></tr>
<tr><td>0F</td><td>0</td><td>SYNC</td><td>Sync processor select. The syncs are obtained by a LPF when HIGH and by the comb filter when LOW.</td></tr>
</table>

Sync Pulse Generator (10)

7	6	5	4	3	2	1	0
STS_7	STS_6	STS_5	STS_4	STS_3	STS_2	STS_1	STS_0

Reg	Bit	Name	Description
10	7-0	STS_{7-0}	**Sync to sync 8 lsbs.** Bottom 8 bits of the number of pixels between sync pulses.

Control Register Definitions (continued)

Sync Pulse Generator (11)

7	6	5	4	3	2	1	0
STB							

Reg	Bit	Name	Description
11	7-0	STB	**Sync to burst.** Controls the number of pixels from sync to burst. This signal starts the burst sample and hold. In SC mode, subtract 25 from the desired delay to generate this value.

Sync Pulse Generator (12)

7	6	5	4	3	2	1	0
BTV							

Reg	Bit	Name	Description
12	7-0	BTV	**Burst to video.** Controls the number of pixels from STB to the start of active video.

Sync Pulse Generator (13)

7	6	5	4	3	2	1	0
AV_7	AV_6	AV_5	AV_4	AV_3	AV_2	AV_1	AV_0

Reg	Bit	Name	Description
13	7-0	AV_{7-0}	**Active video line 8 lsbs.** Bottom 8 bits of the number of pixels during the active video line.

Sync Pulse Generator (14)

7	6	5	4	3	2	1	0
Reserved		AV_9	AV_8	Reserved	STS_{10}	STS_9	STS_8

Reg	Bit	Name	Description
14	7-6	Reserved	**Reserved, set to zero.**
14	5-4	AV_{9-8}	**Active video line 2 msbs.** Two most significant bits of AV.
14	3	Reserved	**Reserved, set to zero.**
14	2-0	STS_{10-8}	**Sync to sync 3 msbs.** Three most significant bits of STS.

Control Register Definitions (continued)

Sync Pulse Generator (15)

7	6	5	4	3	2	1	0
Reserved	VINDO					VDIV	VDOV

Reg	Bit	Name	Description
15	7	Reserved	**Reserved, set to zero.**
15	6-2	VINDO	**Number of lines in vertical window.** The number of lines (0 to 31) after the last EQ pulse that the decoder passes through the Vertical INterval winDOw.
15	1	VDIV	**Action inside VINDO.** The vertical data inside the `VINDO' is passed through a simple decoder when LOW, or is passed unprocessed on the luma channel with the chroma channel set to zero when HIGH.
15	0	VDOV	**Action outside VINDO.** The vertical data after the `VINDO' and before the end of vertical blanking is blanked (YUV = 0) when LOW, or passed through the simple decoder when HIGH.

Sync Pulse Generator (16)

7	6	5	4	3	2	1	0
Reserved		NFDLY		SPGIP		MSIP	

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>16</td><td>7-6</td><td>Reserved</td><td>Reserved, set to zero.</td></tr>
<tr><td>16</td><td>5-4</td><td>NFDLY</td><td>new field detect delay. NTSC frame detect delay:
<table>
<tr><th>NFDLY</th><th>Function</th></tr>
<tr><td>00</td><td>pixel count = 0</td></tr>
<tr><td>01</td><td>pixel count = 1</td></tr>
<tr><td>10</td><td>pixel count = 2</td></tr>
<tr><td>11</td><td>pixel count = 3</td></tr>
</table></td></tr>
<tr><td>16</td><td>3-2</td><td>SPGIP</td><td>SPG input select. Selects the input to the Sync Pulse Generator:
<table>
<tr><th>SPGIP</th><th>Input</th></tr>
<tr><td>00</td><td>External $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$</td></tr>
<tr><td>01</td><td>Digitized sync (subcarrier mode)</td></tr>
<tr><td>10</td><td>TRS words embedded in the D1 data stream</td></tr>
<tr><td>11</td><td>TRS words embedded in the D2 data stream</td></tr>
</table></td></tr>
<tr><td>16</td><td>1</td><td>MSIP</td><td>Mixed sync separator input. Set HIGH for external VIDEOB reference or LOW for output of Low Pass Filter.</td></tr>
<tr><td>16</td><td>0</td><td>SMO</td><td>State Machine Offset. Set HIGH for a 1H offset and LOW for a 0H offset.</td></tr>
</table>

Preliminary Information

Control Register Definitions (continued)

Buffered register set 0 (17) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$SG0_7$	$SG0_6$	$SG0_5$	$SG0_4$	$SG0_3$	$SG0_2$	$SG0_1$	$SG0_0$

Reg	Bit	Name	Description
17	7-0	$SG0_{7-0}$	**Msync gain, 8 lsbs.** Bottom 8 bits of mixed sync scalar lsb = 1/256

Buffered register set 0 (18) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$YG0_7$	$YG0_6$	$YG0_5$	$YG0_4$	$YG0_3$	$YG0_2$	$YG0_1$	$YG0_0$

Reg	Bit	Name	Description
18	7-0	$YG0_{7-0}$	**Y gain, 8 lsbs.** Bottom 8 bits of the luma gain lsb = 1/256

Buffered register set 0 (19) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$UG0_7$	$UG0_6$	$UG0_5$	$UG0_4$	$UG0_3$	$UG0_2$	$UG0_1$	$UG0_0$

Reg	Bit	Name	Description
19	7-0	$UG0_{7-0}$	**U gain, 8 lsbs.** Bottom 8 bits of the U gain lsb = 1/256

Buffered register set 0 (1A) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$VG0_7$	$VG0_6$	$VG0_5$	$VG0_4$	$VG0_3$	$VG0_2$	$VG0_1$	$VG0_0$

Reg	Bit	Name	Description
1A	7-0	$VG0_{7-0}$	**V gain, 8 lsbs.** Bottom 8 bits of the V gain lsb = 1/256

Buffered register set 0 (1B) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
$YG0_9$	$YG0_8$	$UG0_{10}$	$UG0_9$	$UG0_8$	Reserved	$VG0_9$	$VG0_8$

Reg	Bit	Name	Description
1B	7-6	$YG0_{9-8}$	**Y gain, 2 msb.** Top 2 bits of the Y gain. msb = 2
1B	5-3	$UG0_{10-8}$	**U gain, 3 msbs.** Top 3 bits of the U gain. msb = 4
1B	2	Reserved	**Reserved, set to zero.**
1B	1-0	$VG0_{9-8}$	**V gain, 2 msbs.** Top 2 bits of the V gain. msb = 2

Control Register Definitions (continued)

Buffered register set 0 (1C) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
YOFF0$_7$	YOFF0$_6$	YOFF0$_5$	YOFF0$_4$	YOFF0$_3$	YOFF0$_2$	YOFF0$_1$	YOFF0$_0$

Reg	Bit	Name	Description
1C	7-0	YOFF0$_{7-0}$	**Y offset, 8 lsbs.** Bottom 8 bits of luma or RGB offset

Buffered register set 0 (1D) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
Reserved					YOFF0$_8$	SG0$_1$	SG0$_0$

Reg	Bit	Name	Description
1D	7-3	Reserved	**Reserved, set to zero.**
1D	2	YOFF0$_8$	**Y offset, msb.** msb of YOFF
1D	1-0	SG0$_{1-0}$	**Msync gain, 2 msbs.** Top 2 bits of mixed sync scalar. msb = 2

Buffered register set 0 (1E) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
SYSPH0$_7$	SYSPH0$_6$	SYSPH0$_5$	SYSPH0$_4$	SYSPH0$_3$	SYSPH0$_2$	SYSPH0$_1$	VAXIS$_0$

Reg	Bit	Name	Description
1E	7-1	SYSPH0$_{7-1}$	**7 lsbs of phase.** Bottom 7 bits of the system phase offset
1E	0	VAXIS$_0$	**V axis Flip.** The PAL V axis sign bit is flipped when HIGH.

Buffered register set 0 (1F) Active when BUFFER pin set LOW.

7	6	5	4	3	2	1	0
SYSPH0$_{15}$	SYSPH0$_{14}$	SYSPH0$_{13}$	SYSPH0$_{12}$	SYSPH0$_{11}$	SYSPH0$_{10}$	SYSPH0$_9$	SYSPH0$_8$

Reg	Bit	Name	Description
1F	7-0	SYSPH0$_{15-8}$	**8 msbs of phase offset.** Top 8 bits of 15 bit phase offset.

Normalized Subcarrier Frequency (20)

7	6	5	4	3	2	1	0
FSC$_3$	FSC$_2$	FSC$_1$	FSC$_0$	Reserved			

Reg	Bit	Name	Description
20	7-4	FSC$_{3-0}$	**Bottom 4 bits of fsc.** Bottom 4 bits of the 28 bit subcarrier SEED
20	3-0	Reserved	**Reserved, set to zero.**

Control Register Definitions (continued)

Normalized Subcarrier Frequency (21)

7	6	5	4	3	2	1	0
FSC_{11}	FSC_{10}	FSC_9	FSC_8	FSC_7	FSC_6	FSC_5	FSC_4

Reg	Bit	Name	Description
21	7-0	FSC_{11-4}	**Lower 8 bits of fsc.** Lower 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (22)

7	6	5	4	3	2	1	0
FSC_{19}	FSC_{18}	FSC_{17}	FSC_{16}	FSC_{15}	FSC_{14}	FSC_{13}	FSC_{12}

Reg	Bit	Name	Description
22	7-0	FSC_{19-12}	**Middle 8 bits of fsc.** Middle 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (23)

7	6	5	4	3	2	1	0
FSC_{27}	FSC_{26}	FSC_{25}	FSC_{24}	FSC_{23}	FSC_{22}	FSC_{21}	FSC_{20}

Reg	Bit	Name	Description
23	7-0	FSC_{27-20}	**Top 8 bits of fsc.** Top 8 bits of the 28 bit subcarrier SEED

Normalized Subcarrier Frequency (24-25)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
24-25	7-0	Reserved	**Reserved, set to zero.**

Preliminary Information

Control Register Definitions (continued)

Output Format Control (26)

7	6	5	4	3	2	1	0
Reserved		LDVIO	OPCKS	DPCEN	DPC		

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>26</td><td>7-6</td><td>Reserved</td><td>Reserved, set to zero.</td></tr>
<tr><td>26</td><td>5</td><td>LDVIO</td><td>LDV clock select. LDV is an output when LOW and an input when HIGH</td></tr>
<tr><td>26</td><td>4</td><td>OPCKS</td><td>Output clock select. The output data are clocked by the CLOCK pin when LOW and by the LDV pin when HIGH.</td></tr>
<tr><td>26</td><td>3</td><td>DPCEN</td><td>DPC enable. When HIGH on the TMC22153, the Decoder Product Code is enabled: a value written into DPC determines the decoder product emulated by the TMC22153. In all other versions of the decoder, DPC is read-only, and returns the code of the particular encoder version installed.</td></tr>
<tr><td>26</td><td>2-0</td><td>DPC</td><td>Decoder product code
<table>
<tr><th>DPC</th><th>Function</th></tr>
<tr><td>000</td><td>Reserved</td></tr>
<tr><td>001</td><td>TMC22051</td></tr>
<tr><td>010</td><td>TMC22052</td></tr>
<tr><td>011</td><td>TMC22053</td></tr>
<tr><td>100</td><td>Reserved</td></tr>
<tr><td>101</td><td>TMC22151</td></tr>
<tr><td>110</td><td>TMC22152</td></tr>
<tr><td>111</td><td>TMC22153</td></tr>
</table>
Read/Write in the TMC22153 only. Read-only in all other devices.</td></tr>
</table>

Buffered register set 1 (27) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$SG1_7$	$SG1_6$	$SG1_5$	$SG1_4$	$SG1_3$	$SG1_2$	$SG1_1$	$SG1_0$

Reg	Bit	Name	Description
27	7-0	$SG1_{7-0}$	**Msync gain, 8 lsbs.** Bottom 8 bits of mixed sync scalar lsb = 1/256

Buffered register set 1 (28) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
$YG1_7$	$YG1_6$	$YG1_5$	$YG1_4$	$YG1_3$	$YG1_2$	$YG1_1$	$YG1_0$

Reg	Bit	Name	Description
28	7-0	$YG1_{7-0}$	**Y gain, 8 lsbs.** Bottom 8 bits of the luma gain lsb = 1/256

Control Register Definitions (continued)

Buffered register set 1 (29) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
UG1$_7$	UG1$_6$	UG1$_5$	UG1$_4$	UG1$_3$	UG1$_2$	UG1$_1$	UG1$_0$

Reg	Bit	Name	Description
29	7-0	UG1$_{7-0}$	**U gain, 8 lsbs.** Bottom 8 bits of the U gain lsb = 1/256

Buffered register set 1 (2A) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
VG1$_7$	VG1$_6$	VG1$_5$	VG1$_4$	VG1$_3$	VG1$_2$	VG1$_1$	VG1$_0$

Reg	Bit	Name	Description
2A	7-0	VG1$_{7-0}$	**V gain, 8 lsbs.** Bottom 8 bits of the V gain lsb = 1/256

Buffered register set 1 (2B) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
YG1$_9$	YG1$_8$	UG1$_{10}$	UG1$_9$	UG1$_8$	Reserved	VG1$_9$	VG1$_8$

Reg	Bit	Name	Description
2B	7-6	YG1$_{9-8}$	**Y gain, 2 msbs.** Top 2 bits of the Y gain msb = 2
2B	5-3	UG1$_{10-8}$	**U gain, 3 msbs.** Top 3 bits of the U gain. msb = 4
2B	2	Reserved	**reserved, set to zero**
2B	1-0	VG1$_{9-8}$	**V gain, 2 msbs.** Top 2 bits of the V gain msb = 2

Buffered register set 1 (2C) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
YOFF1$_7$	YOFF1$_6$	YOFF1$_5$	YOFF1$_4$	YOFF1$_3$	YOFF1$_2$	YOFF1$_1$	YOFF1$_0$

Reg	Bit	Name	Description
2C	7-0	YOFF1$_{7-0}$	**Y offset, 8 lsbs.** Bottom 8 bits of luma or RGB offset

Control Register Definitions (continued)

Buffered register set 1 (2D) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
Reserved					YOFF1$_8$	SG1$_7$	SG1$_0$

Reg	Bit	Name	Description
2D	7-3	Reserved	**Reserved, set to zero.**
2D	2	YOFF1$_8$	**Y offset, msb.** msb of YOFF
2D	1-0	SG1$_{7,0}$	**Msync gain, 2 msbs.** Top 2 bits of mixed sync scalar msb = 2

Buffered register set 1 (2E) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
SYSPH1$_7$	SYSPH1$_6$	SYSPH1$_5$	SYSPH1$_4$	SYSPH1$_3$	SYSPH1$_2$	SYSPH1$_1$	SYSPH1$_0$

Reg	Bit	Name	Description
2E	7-1	SYSPH1$_{7-0}$	**8 lsbs of phase.** Bottom 8 bits of the system phase offset
2E	0	VAXIS$_0$	**V axis Flip.** The PAL V axis sign bit is flipped when HIGH.

Buffered register set 1 (2F) Active when BUFFER pin set HIGH.

7	6	5	4	3	2	1	0
SYSPH1$_{15}$	SYSPH1$_{14}$	SYSPH1$_{13}$	SYSPH1$_{12}$	SYSPH1$_{11}$	SYSPH1$_{10}$	SYSPH1$_9$	SYSPH1$_8$

Reg	Bit	Name	Description
2F	7-0	SYSPH0$_{15-0}$	**8 msbs of phase offset.** Top 8 bits of 15 bit phase offset.

Preliminary Information

Control Register Definitions (continued)

Video Measurement (30)

7	6	5	4	3	2	1	0
Reserved	LGF	LGEN	LGEXT	RESERVED	PGG	PGEN	PGEXT

Reg	Bit	Name	Description
30	7	Reserved	**Reserved, set to zero.**
30	6	LGF	**Line grab flag.** Set HIGH when the decoder has grabbed a line, and must be reset LOW before another line can be grabbed.
30	5	LGEN	**Line grab enable.** When HIGH, the line grabber is used to freeze the contents of the line store, at the programmed line and field count. The phase and frequency of the frozen line are also stored from the DRS, and are continually used to reset the DDS, once per line, until LGF is set LOW. When LGEN is LOW, the line freeze is disabled, the internal loops operate normally, and the line grab signal is used only to gate the pixel grab.
30	4	LGEXT	**Ext line grab enable.** The SET pin is used to produce the line grabber pulse when HIGH and the internal line decode is used when LGEXT is LOW.
30	3	Reserved	**Reserved, set to zero.**
30	2	PGG	**Pixel grab gate.** When HIGH the pixel grab is gated by the field and line grab signals to enable one pixel per four fields in NTSC and 8 field in PAL to be grabbed. This function is disabled if PGEN is set LOW.
30	1	PGEN	**Pixel grab enable.** When HIGH the 10 bit G/Y, B/U, and R/V data, and the mixed sync and luma data after the comb filter, and the demodulated (B-Y) and (R-Y) color difference signals are grabbed once every line at the programmed pixel grab number. When LOW the contents of the pixel grab registers are held and the pixel grab pulse is ignored.
30	0	PGEXT	**Ext pixel grab enable.** The SET pin is used to produce the pixel grab pulse when HIGH and the internal pixel decode is used when PGEXT is LOW.

Video Measurement (31)

7	6	5	4	3	2	1	0
PG_7	PG_6	PG_5	PG_4	PG_3	PG_2	PG_1	PG_0

Reg	Bit	Name	Description
31	7-0	PG_{7-0}	**Pixel grab, 8 lsbs.** Bottom 8 bits of the pixel grab.

Video Measurement (32)

7	6	5	4	3	2	1	0
LG_7	LG_6	LG_5	LG_4	LG_3	LG_2	LG_1	LG_0

Reg	Bit	Name	Description
32	7-0	LG_{7-0}	**Line grab, 8 lsbs.** Bottom 8 bits of the line grab.

Control Register Definitions (continued)

Video Measurement (33)

7	6	5	4	3	2	1	0
Reserved	FG			LG_8	PG_{10}	PG_9	PG_8

Reg	Bit	Name	Description
33	7	Reserved	**Reserved.**
33	6-4	FG	**Field grab number.** Field grab number
33	3	LG_8	**Msb of line grab.** msb of line grab
33	2-0	PG_{10-8}	**Pixel grab, 3 msbs.** 3 msbs of pixel grab

Registers 34-3C are Read-Only

Register (34)

7	6	5	4	3	2	1	0
GY_9	GY_8	GY_7	GY_6	GY_5	GY_4	GY_3	GY_2

Reg	Bit	Name	Description
34	7-0	GY_{9-2}	**G/Y grab, 8 msbs.** Top 8 bits of the "grabbed" G/Y data

Register (35)

7	6	5	4	3	2	1	0
BU_9	BU_8	BU_7	BU_6	BU_5	BU_4	BU_3	BU_2

Reg	Bit	Name	Description
35	7-0	BU_{9-2}	**B/U grab, 8 msbs.** Top 8 bits of the "grabbed" B/U data

Register (36)

7	6	5	4	3	2	1	0
RV_9	RV_8	RV_7	RV_6	RV_5	RV_4	RV_3	RV_2

Reg	Bit	Name	Description
36	7-0	RV_{9-2}	**R/V grab, 8 msbs.** Top 8 bits of the "grabbed" R/V data

Register (37)

7	6	5	4	3	2	1	0
Reserved		GY_1	GY_0	BU_1	BU_0	RV_1	RV_0

Reg	Bit	Name	Description
37	7-6	Reserved	**Reserved.**
37	5-4	GY_{1-0}	**G/Y grab, 2 lsbs.** Bottom two bits of G/Y data
37	3-2	BU_{1-0}	**B/U grab, 2 lsbs.** Bottom two bits of B/U data
37	1-0	RV_{1-0}	**R/V grab, 2 lsbs.** Bottom two bits of R/V data

Control Register Definitions (continued)

Register (38)

7	6	5	4	3	2	1	0
Y_9	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2

Reg	Bit	Name	Description
38	7-0	Y_{9-2}	**Luma grab, 8 msbs.** Top 8 bits of the "grabbed" luma data after YPROC

Register (39)

7	6	5	4	3	2	1	0
M_9	M_8	M_7	M_6	M_5	M_4	M_3	M_2

Reg	Bit	Name	Description
39	7-0	M_{9-2}	**Msync grab, 8 msbs.** Top 8 bits of the "grabbed" mixed sync data after YPROC

Register (3A)

7	6	5	4	3	2	1	0
U_9	U_8	U_7	U_6	U_5	U_4	U_3	U_2

Reg	Bit	Name	Description
3A	7-0	U_{9-2}	**U grab, 8 msbs.** Top 8 bits of the "grabbed" U data

Register (3B)

7	6	5	4	3	2	1	0
V_9	V_8	V_7	V_6	V_5	V_4	V_3	V_2

Reg	Bit	Name	Description
3B	7-0	V_{9-2}	**V grab, 8 msbs.** Top 8 bits of the "grabbed" V data

Register (3C)

7	6	5	4	3	2	1	0
Y_1	Y_0	M_1	M_0	U_1	U_0	V_1	V_0

Reg	Bit	Name	Description
3C	7-6	Y_{1-0}	**Luma grab, 2 lsbs.** Bottom 2 bits of luma data
3C	5-4	M_{1-0}	**Msync grab, 2 lsbs.** Bottom 2 bits of mixed sync data
3C	3-2	U_{1-0}	**U grab, 2 lsbs.** Bottom 2 bits of U data
3C	1-0	V_{1-0}	**V grab, 2 lsbs.** Bottom 2 bits of V data

Control Register Definitions (continued)

Test Control (3D-3F)

7	6	5	4	3	2	1	0
TEST							

Reg	Bit	Name	Description
3D-3F	7-0	TEST	**Must be set to zero.** Auto increment stops at 3F

Status - Read Only (40)

7	6	5	4	3	2	1	0
DDSPH							

Reg	Bit	Name	Description
40	7-0	DDSPH	**DDS phase, 8 msbs.** The top 8 bits of the sine data generated in the internal DDS.

Status - Read Only (41)

7	6	5	4	3	2	1	0
LINEST	BGST	VACT2	PALODD	VFLY	FGRAB	LGRAB	PGRAB

Reg	Bit	Name	Description
41	7	LINEST	**Pixel count reset.** Pixel count reset
41	6	BGST	**Start of burst gate.** Start of burst gate
41	5	VACT2	**Half line flag.** Half line flag
41	4	PALODD	**PAL Ident.** PAL Ident (low on NTSC lines)
41	3	VFLY	**Vertical count reset.** Vertical count reset
41	2	FGRAB	**Field grab.** Field grab
41	1	LGRAB	**Line grab.** Line grab
41	0	PGRAB	**Pixel grab.** Pixel grab

Status - Read Only (42)

7	6	5	4	3	2	1	0
FLD	$\overline{\text{VBLK}}$	$\overline{\text{HBLK}}$	LID				

Reg	Bit	Name	Description
42	7	FLD	**Field flag (F in D1 output).** Field flag (F in D1 output)
42	6	$\overline{\text{VBLK}}$	**Vertical blanking (V in D1 output).** Vertical blanking (V in D1 output)
42	5	$\overline{\text{HBLK}}$	**Horizontal blanking (H in D1 output).** Horizontal blanking (H in D1 output)
42	4-0	LID	**Line identification.** Line identification

Control Register Definitions (continued)

Status - Read Only (43)

7	6	5	4	3	2	1	0
YGO	YGU	UBO	UBU	VRO	VRU	Reserved	

Reg	Bit	Name	Description
43	7	YGO	**Y/G overflow.** Y/G overflow
43	6	YGU	**Y/G underflow.** Y/G underflow
43	5	UBO	**C_B/B overflow.** C_B/B overflow
43	4	UBU	**C_B/B underflow.** C_B/B underflow
43	3	VRO	**C_R/R overflow.** C_R/R overflow
43	2	VRU	**C_R/R underflow.** C_R/R underflow
43	1-0	Reserved	**Reserved.**

Status - Read Only (44)

7	6	5	4	3	2	1	0
MONO	FPERR						

Reg	Bit	Name	Description
44	7	MONO	**Color kill flag.** High when burst detected and LOW when monochrome signal is detected.
44	6-0	FPERR	**Frequency/Phase error.** Top 7 bits of the modulo two pi frequency or phase error. Reported once per line.

Status - Read Only (45)

7	6	5	4	3	2	1	0
DRS							

Reg	Bit	Name	Description
45	7-0	DRS	**DRS signal.** The 8-bit Decoder Reference Signal.

Status - Read Only (46)

7	6	5	4	3	2	1	0
PARTID							

Reg	Bit	Name	Description
46	7-0	PARTID	**Part family ID.** Reads back the 8-bit part ID number. Read-only. Returns CDh.

Control Register Definitions (continued)

Status - Read Only (47)

7	6	5	4	3	2	1	0
REVID							

Reg	Bit	Name	Description
47	7-0	REVID	**Revision number.** The 8-bit chip revision number.

Status - Read Only (48-4A)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
48-4A	7-0	Reserved	**Reserved.**

Status - Read Only (4B)

7	6	5	4	3	2	1	0
$\overline{\text{PKILL}}$	CFSTAT		XOP				

<table>
<tr><th>Reg</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>4B</td><td>7</td><td>$\overline{\text{PKILL}}$</td><td>Phase kill from comb fail. Phase kill from comb fail.</td></tr>
<tr><td>4B</td><td>6-5</td><td>CFSTAT</td><td>Comb filter status. Comb filter status.
<table>
<tr><th>CFSTAT</th><th>STATUS</th></tr>
<tr><td>00</td><td>3 tap comb</td></tr>
<tr><td>01</td><td>3 tap [lower] comb</td></tr>
<tr><td>10</td><td>3-tap [upper] comb</td></tr>
<tr><td>11</td><td>2 tap comb</td></tr>
</table></td></tr>
<tr><td>4B</td><td>4-0</td><td>XOP</td><td>XLUT output. XLUT output.</td></tr>
</table>

Status - Read Only (4C-FF)

7	6	5	4	3	2	1	0
Reserved							

Reg	Bit	Name	Description
4C-FF	7-0	Reserved	**Reserved.**

Decoder Introduction

All composite video decoders perform fundamentally the same operation. The first stage is to separate the luminance and chrominance. The second stage is to lock the internally generated sine and cosine waveforms to the burst on the decoded chrominance signal, demodulate, and then filter the chrominance signal to produce the color difference signals. The last stage either scales the luminance and color difference signals, or converts them into red, green, and blue component video signals. These three stages are shown in Figure 3.

The complete separation of composite video signals into pure luminance (luma) and chrominance (chroma) signals is practically impossible, especially when the input source contains intraframe motion. Therefore, the luminance (luma) signal will generally contain some high frequency chrominance, termed *cross luma*, and the chroma signal will contains some of the high frequency luma signal, centered around the subcarrier frequency, termed *cross color.*
The degree of cross luma and cross color is directly proportional to the filter used for the YC separation, the picture content, and the complexity of any post processing of the decoded signals.

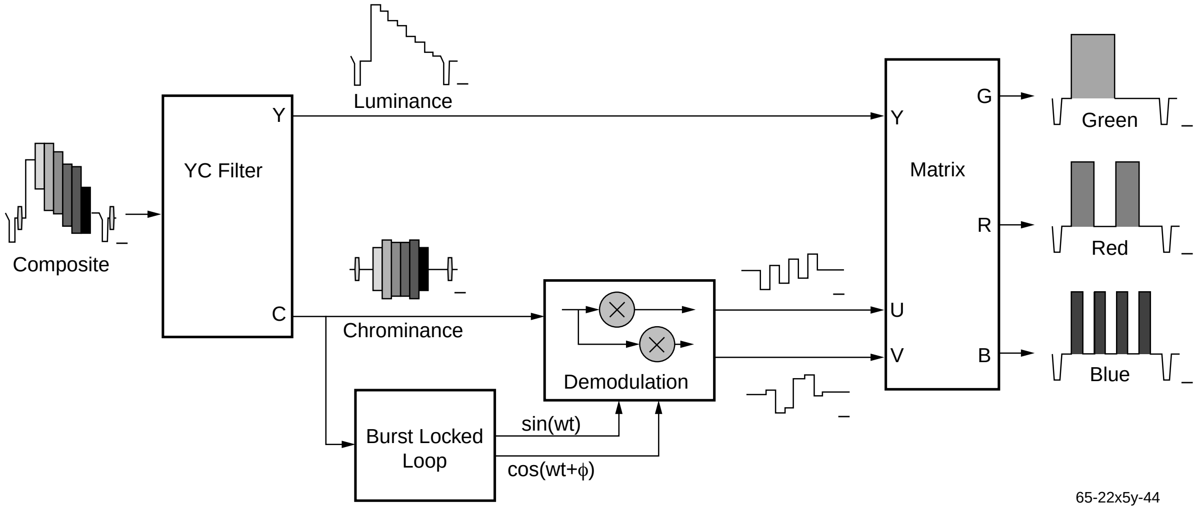


Figure 3. Fundamental Decoder Block Diagram

YC Separation

The relationship between the chrominance and luminance bandwidths is shown for both PAL and NTSC in Figure 4, wherein the shaded area denotes the part of the composite video frequency spectrum shared by both the chrominance and high frequency luminance signals.

The *Luma Notch and Chroma Bandpass* Technique for YC Separation

The simplest method of separating these chrominance and luminance signals, is to assume the chroma bandwidth is limited to a few hundred kilohertz around the subcarrier frequency. In this case a notch filter designed to remove just these frequencies from the composite video frequency spectrum provides the luma signal, while a bandpass filter

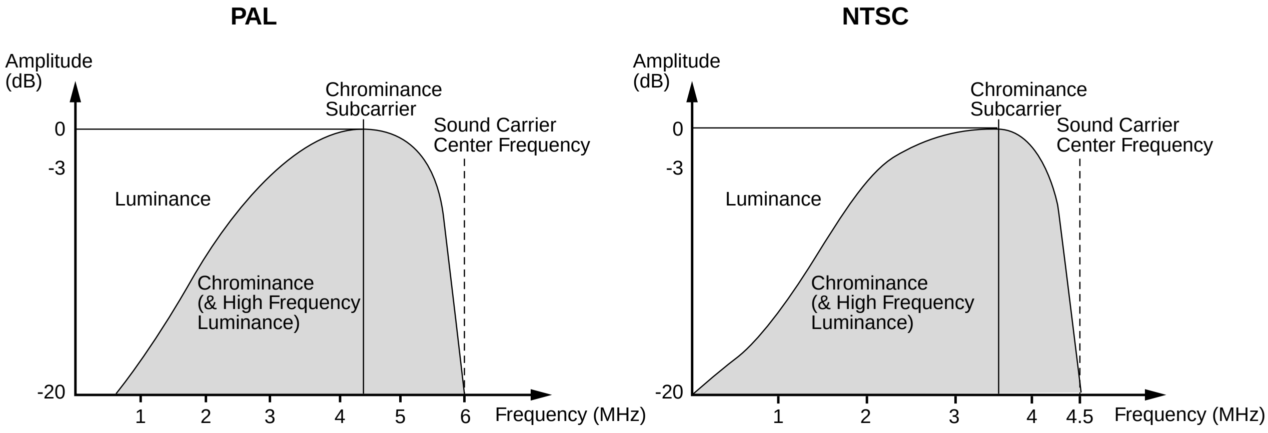


Figure 4. Comparison of the Frequency Spectrum of NTSC and PAL Composite Video Signals

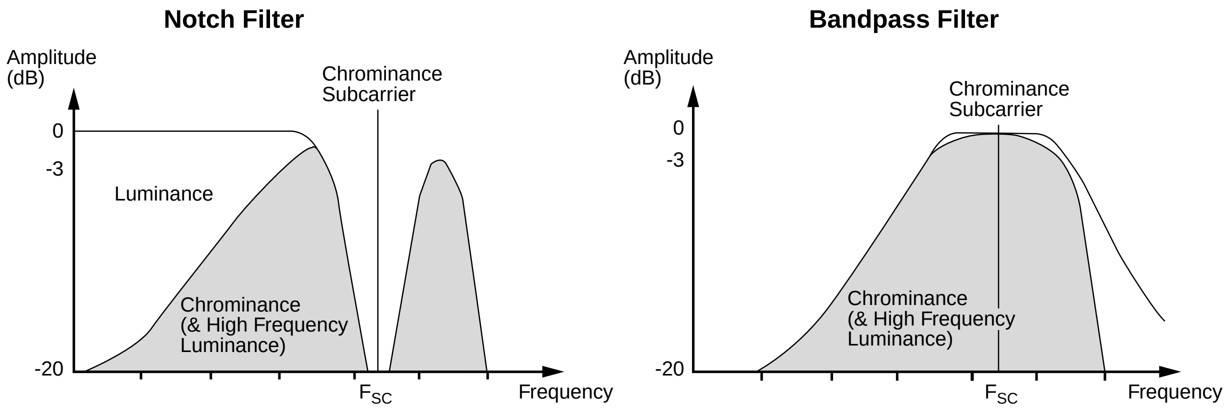


Figure 5. Examples of Notch and Bandpass Filters

centered at the subcarrier frequency produces the chroma signal. This simple technique works well in pictures containing large flat areas of color, however this is rarely the case. If, as is generally true, the picture contains high frequency luma and chroma transitions, for example herring bone suit jackets, branches of trees, text, etc., cross color and cross luma artifacts are evident.

The presence of cross color or cross luma is generally acceptable when viewing the decoded picture on a monitor from several feet, as would be the case in most homes on commercial television sets. However, these artifacts become increasingly difficult to process, or ignore, when the image is to be compressed or manipulated. In these cases more sophisticated methods of separating the luma and chroma signals, such as frame, field, or line based comb filter decoders, are required.

Another important disadvantage of the “luma notch filter and bandpass chroma” technique is that once a notch filter has been used on the luminance channel this portion of the luminance frequency spectrum is lost. This effect becomes increasingly objectionable if the decoder component outputs are subsequently re-encoded into a composite video signal.

Comb Filter Architectures for YC Separation

A comb filter uses the relationship between the number of subcarrier cycles per line period, to cancel the chrominance signal over multiple line periods. This is shown for an NTSC two line comb filter in Figure 6. In NTSC there a 227.5 subcarrier cycles per line period, therefore the subcarrier can be canceled by simply adding two consecutive field scan lines. In PAL(B/I/ etc.) there are 283.7516 subcarrier cycles per line period, ignoring the 0.0016 cycle advance caused by the 25Hz offset, the PAL subcarrier can be canceled by adding the first and third line of three consecutive field scan lines. Due to the 270 degree advance, it is not possible to use information from consecutive field lines without adding a PAL modifier. A PAL modifier produces a 90 degree phase shift in the chrominance signal by multiplying the chrominance signal by a signal at two times the subcarrier frequency that is phased locked to the subcarrier burst reference in the composite video waveform. In addition the PAL modifier inverts the V component of the chrominance signal. This document refers to line based comb decoders when discussing decoders that use inputs from sequential scan lines, i.e. lines from the same field, field based comb decoders when describing decoders that use inputs from sequential fields, and finally frame based comb decoders when examining decoders that use inputs from sequential frames.

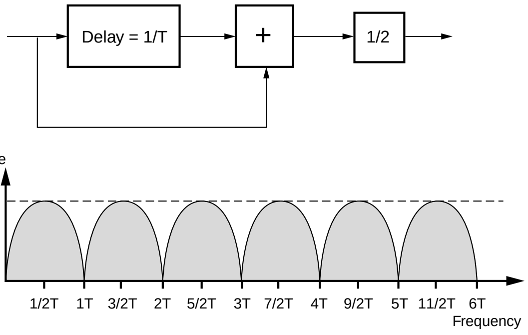


Figure 6.

Composite Line-Based Comb Decoders

The phase relationship of the quadrature modulated chrominance signal can also be represented as in Figure 7. The three line comb based decoder is clearly biased towards 1H which illustrates the inherent one line delay through a 3 line comb, while a two line comb based decoder is biased towards 0H. In the following discussions a flat color represents video of constant luma and chroma magnitude and phase.

In NTSC, adding two adjacent lines of flat color will cancel the chroma and leave the luma whereas subtracting two lines of flat color will cancel the luma and leave the chroma. In a 3 line comb filter the flat color on 0H and 2H is added to provide the flat color average before adding or subtracting from 1H.

In PAL, adding the flat color from 0H and 2H will cancel the chroma and leave the luma while subtracting the flat color from 0H and 2H will cancel the luma and leave the chroma. However, chroma generated in this manner has no simple phase relationship to the chroma on 1H. Therefore normally 0H and 2H are added together to produce the average luma across 3 lines and this is then subtracted from 1H to produce the combed chroma.

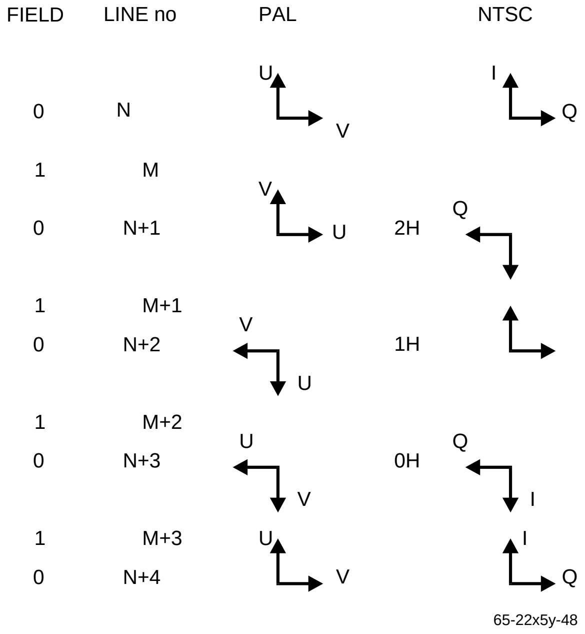


Figure 7. Chrominance Vector Rotation in PAL and NTSC

YC Line-Based Comb Filters

The luminance and chrominance signals, are by definition, already separated for YC inputs. However, if the original source was composite, there is a distinct possibility that there is some residual luminance (cross color) in the chrominance signal and some residual chrominance (cross luma) in the luminance signal. It is therefore legitimate to treat these signals as if they were simply the output from bandsplit filters and process the luma and chroma signals accordingly.

D1 Line-Based Comb Filters

A D1 data stream consists of multiplexed Y, C_b and C_R component data. If the original source was composite there maybe luminance (cross color) in C_BC_R and chrominance (cross luma) in Y. In the first case any luminance that was passed through a demodulator along with the chroma to produce the baseband C_BC_R color difference signals would have the same characteristics as chroma. That is to say, the cross color would advance by 180° every line in NTSC and every 2 lines in PAL. It is therefore possible to remove this cross color in a comb filter. In the latter case any chrominance that is still in the Y data can obviously be removed in a comb filter as well.

The original source for the D1 signal could also have been computer graphics. In this case, the comb filter can be used to remove the picture flicker and convert the output to RGB.

NTSC Frame and Field Based Decoders

Composite Frame-Based Comb Filters

In NTSC the chrominance vectors advance by 180 degrees every line, therefore after 525 lines the 2 adjacent frame lines 0H and FR0H and the two consecutive field lines FR0H and FR1H are 180 degrees apart. The flat color on FR0H and FR1H can be added or subtracted to provide the luminance or chrominance to subtract from 0H.

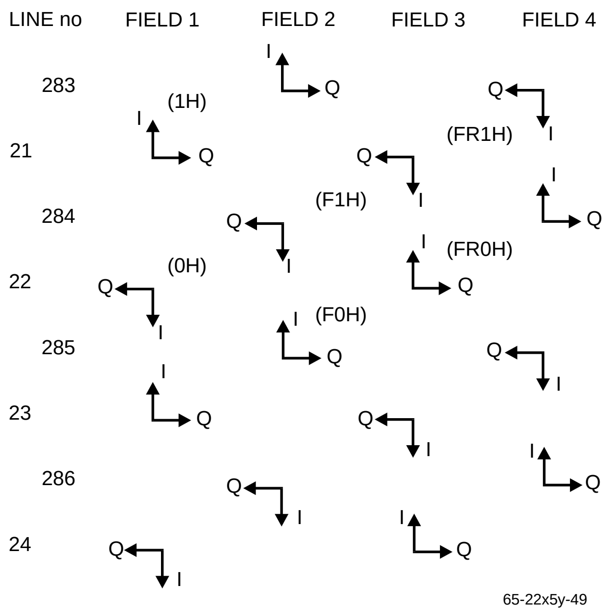


Figure 8. Chrominance Vector Rotation Over 4 Fields in NTSC

Composite Field-Based Comb Filters

In NTSC field based comb decoders, there is an external delay of 263 lines, therefore the 2 adjacent picture lines 0H and F0H and the two consecutive field lines F0H and F1H are 180 degrees apart. The flat color on F0H and F1H can be added or subtracted to provide the luminance or chrominance to subtract from 0H.

PAL Frame- and Field-Based Decoders

Composite PAL Frame-Based Comb Filters

In PAL the chrominance vectors advance by 270 degrees every line. After 625 lines the two adjacent frame lines 0H and FR0h are 90 degrees apart. It is therefore necessary to delay the FR0H data by an addition line so that 0H and FR0H are 180 degrees apart. The flat color on 0H and FR0H can now be added to provide the luminance or subtracted to produce chrominance.

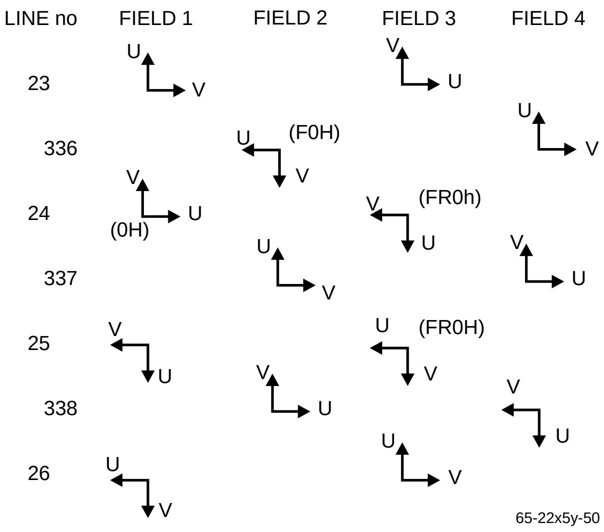


Figure 9. Chrominance Vector Rotation Over 4 Fields in PAL

In fields 5, 6, 7, and 8 the U and V vectors are 180 degrees advanced from fields 1, 2, 3, and 4.

Composite, PAL Field-Based Comb Filters

In PAL field based comb decoders, there is an external delay of 312 lines, therefore the 2 adjacent picture lines 0H and F0H are 180 degrees apart. In fields 5, 6, 7, and 8 the U and V vectors are 180 degrees advanced from fields 1, 2, 3, and 4.

The TMC22x5y Comb Filter Architecture

The TMC22x5y, when implementing a line based comb filter, has a core architecture as shown in Figure 10. The concept of the complementary bandsplit filter is also observed in the complementary comb filter architecture. It is therefore possible to adapt between the complementary comb filter and bandsplit filter without throwing away any of the original composite video frequency spectrum.

The first step in the complementary comb filter is to separate the high frequency luminance from the chrominance signal. This combed high frequency luma signal is shown as *YCOMB* in Figure 10. The second step is to produce an array of comb filter error signals that indicate the degree of confidence that the *YCOMB* signal is just the high frequency luma and not a combination of high frequency luma and chroma smeared over the number of lines used in the comb filter. The signal representing this degree of confidence is termed “K” in Figure 10. The last step is to provide a complementary cross fade between the *YCOMB* signal and the output of the complementary bandsplit filter, shown as *SIMPLE* in Figure 10. The *FLAT* signal is simply a delayed version of the input to the comb filter, therefore the sum of *Output1* and *Output2* will always be equal to the *FLAT* video input.

The TMC22x53 comb filter architecture has three taps. These taps are three consecutive field lines in a line based comb, three consecutive picture lines in a field based comb, or lines that are one frame and one field line apart in the frame based comb. In addition to these different inputs to the comb filter, NTSC and PAL video signals comb over different taps in different architectures, as described in the comb filter introduction.

The total internal pipeline latency is 1H + 38 pixels for 3 line comb filters, for all other comb filter and simple decoder architectures the pipeline latency is 38 pixels.

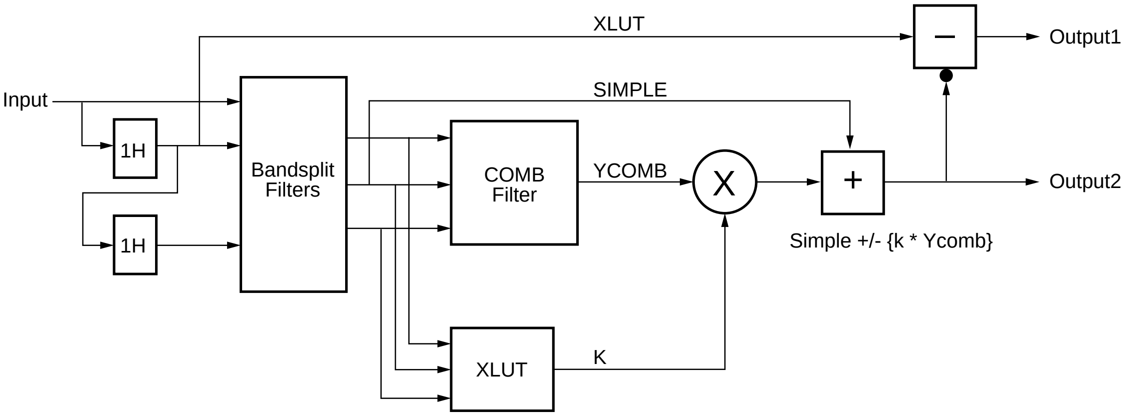


Figure 10. TMC22x5y Line Based Comb Filter Architecture

TMC22x5y Functional Description

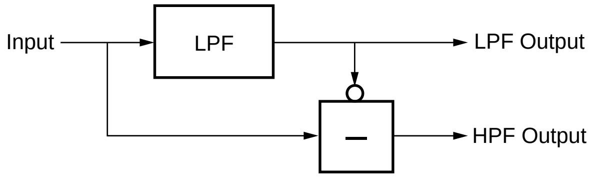
Input Processor

The input processor selects between the two external video sources on VIDEO A and VIDEO B. If the TRS stripper or GRS stacker is active, then the user must select the input with either the GRS (in genlock mode) or with the embedded TRS words as output VA. If the input data are separate luma and chroma or Y and C_BC_R data the input processor must be programmed to put the chrominance or C_BC_R onto output VB and the luminance or Y onto VA.

To ensure that the chrominance data or the C_BC_R data are in two's complement arithmetic format, the register bit MSBI inverts the msb of the DB input. For composite inputs, the IPCMSB register bit should be set LOW, as the ABMUX register bit is used to select the input(s) to the comb filter.

Bandsplit Filter (BSF)

In its simple mode of operation, the TMC22x5y uses a complementary bandsplit filter, instead of a notch filter for the luma and a bandpass for the chroma. The notch and bandpass filter technique, removes frequency bands from the composite video spectrum which can never be retrieved. The complementary bandsplit filter technique, shown in Figure 12, allows the decoded component video signals to be re-encoded into a composite video signal with the minimum of losses to the composite video spectrum.

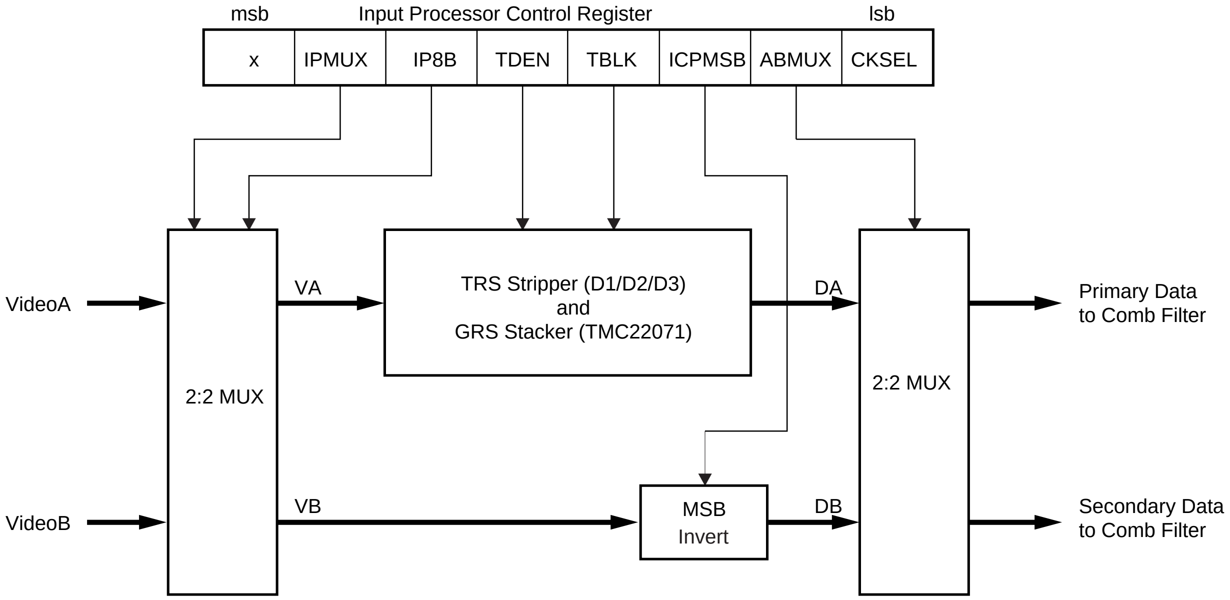


65-22x5y-53

Figure 12. Complementary Bandsplit Filter

The complementary bandsplit filter separates the base band composite video into two bands by passing it through a low pass filter and subtracting the low pass (luma) data from the composite video to produce the high pass (chroma) data. As the base bandwidths and subcarrier frequencies of the different NTSC and PAL video formats are so different, and the decoder has to be capable of working over a large frequency range, it is necessary to provide two low pass filters. These filters are selectable by the BSFSEL register bit and are independent of the video standard. A comparison of the different data rates to normalized subcarrier frequencies is provided in Table 2.

The complementary bandsplit low pass frequency response is shown in Figure 13 and Figure 14.



65-22x5y-52

Figure 11. Input Processor

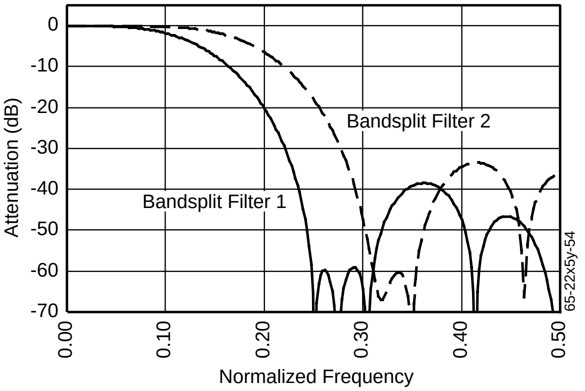


Figure 13. Bandsplit Filter, Full Frequency Response

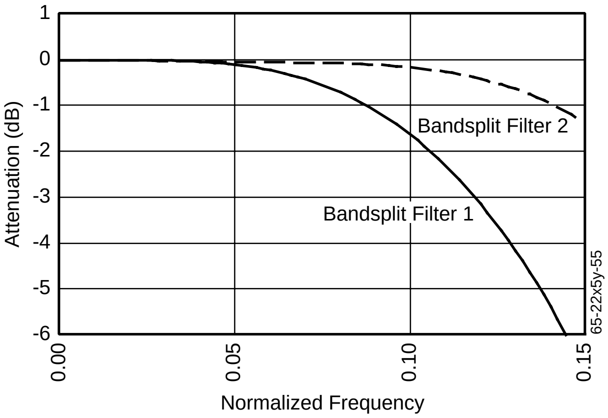


Figure 14. Bandsplit Filter, Passband Response

Table 2. Normalized Subcarrier Frequency as a Function of Pixel Data Rates

Pixel Rate (MHz)	F_{SC} (MHz)	Normalized F_{SC}	Comments
12.27	3.57954545	0.2917	NTSC square pixel rate
13.50	3.57954545	0.2652	NTSC D1 pixel rate
13.50	4.43361875	0.3284	PAL-I D1 pixel rate
14.32	3.57954545	0.2500	NTSC four times subcarrier (D2/D3)
14.75	4.43361875	0.3006	PAL-I square pixel rate
15.00	4.43361875	0.2956	PAL-I square pixel rate
17.73	4.43361875	0.2500	PAL-I four times subcarrier (D2/D3)
13.5	3.57561149	0.2649	PAL-M D1 pixel rate
13.5	3.58205625	0.2653	PAL-N D1 pixel rate
14.30	3.57561149	0.2500	PAL-M four times subcarrier (D2/D3)

Comb Filter Input

The inputs to the comb filter are selected from either the high frequency outputs of the bandsplit filters, if using a chroma comb filter, or the full composite waveforms when implementing a luma comb. The two sets of high and low frequency signals from the bandsplit filters are used for both the luma and chroma *SIMPLE* signals, and in the generation of the comb fail signals. These signals are denoted xHL, xHH, and xHF where L denotes the low frequency portion of the signal, H the high frequency portion of the signal and F the full frequency spectrum of the input signal from line x; and are shown in Figure 15.

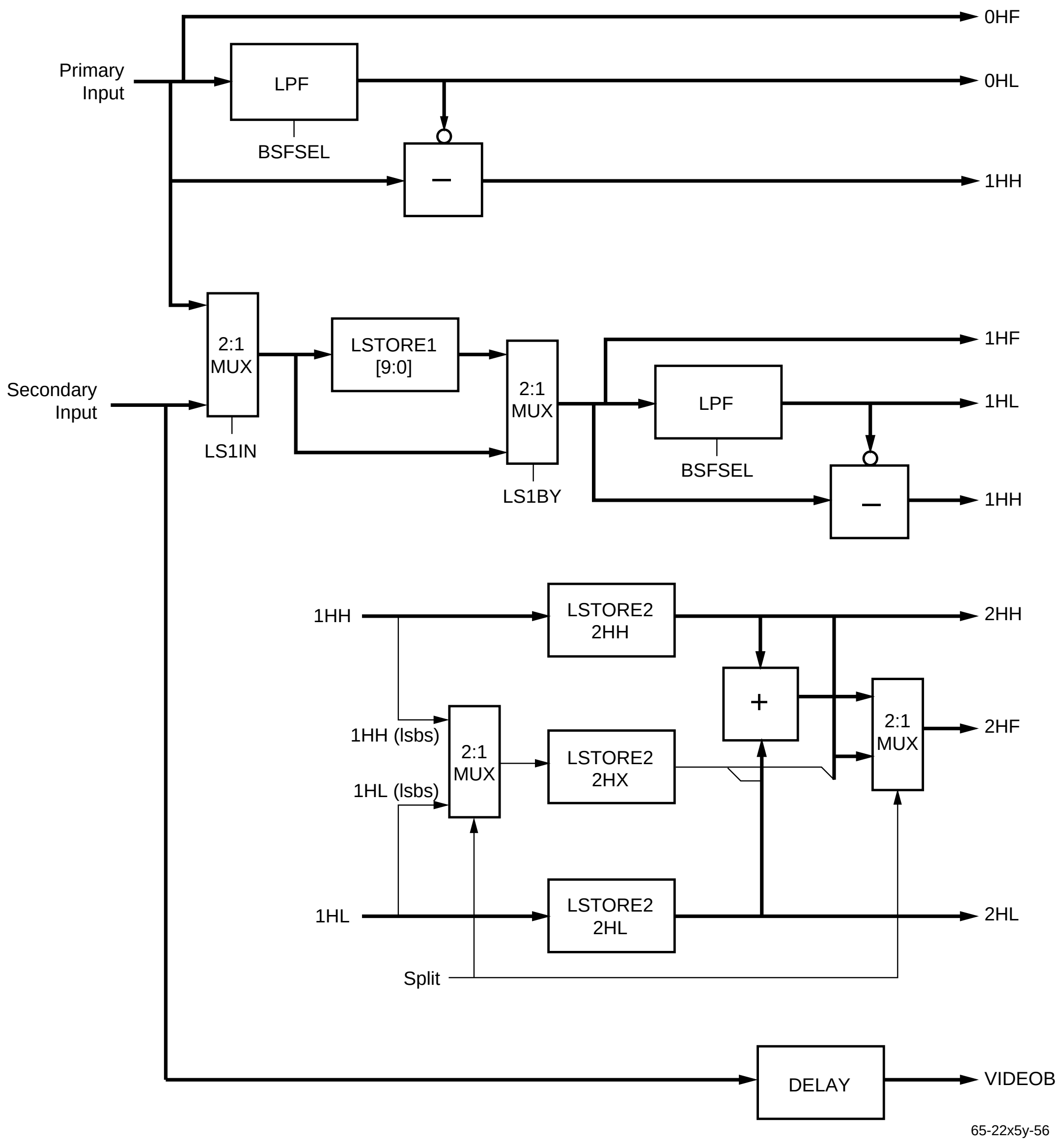


Figure 15. Block Diagram of Comb Filter Input

The primary and secondary inputs are selected within the input processor. The primary input is normally the undelayed composite video signal in line, field, and frame based comb filters or either the luma or chroma channel when processing YC or D1 signals. The secondary provides the field or frame delayed composite input for field and frame based comb filters and the chroma or luma channel when processing YC or D1 signals.

When implementing a line based comb filter the outputs of 1H bandsplit filter, ie 1HH, 1HL, are delayed through the second line store, LSTORE2. The number of bits delayed is dependent upon the type of comb filter being implemented. For chroma comb filters all the bits of the 1HH signal are delayed, as this information supplies the outer tap of the chroma comb filter, while only the upper bits of 1HL are delayed as this data is used only in the generation of the luma error signals. In the case of luma combs an equal number of bits of the 1HH and 1HL signals are delayed and summed together to produce the 2HF signal for the outer tap of the luma comb filter. The configuration of LSTORE2 is determined by the SPLIT register bit.

It is important to note that when implementing a field or frame based comb filter the secondary input must be selected by setting the LSIN register bit HIGH, and the first line store, LSTORE1, must be bypassed by setting the LS1BY register bit HIGH.

For YC and D1 processing the secondary input bypasses the comb filter completely and provides the VIDEOB signal input the 3:1 multiplexer used to select the FLAT signal, see Figure 16.

Adaptive Comb Filter

The IPCF[1:0] register bits select the inputs to the adaptive comb filter, this would normally be xHH for chroma combs, xHF for luma combs, and xHL if the luminance signal was to be sampled dropped on the output of the TMC22x5y. The Gaussian filters in the sample drop mode already limit the chrominance bandwidth to 1.3MHz allowing a [2:1:1] data format on the output, with the luminance signal having been vertically filtered by a fixed 3 line comb filter.

The SIMP selection bit is an internally generated signal based upon the comb filter selected. If a 3 line chroma, luma, or D1 comb filter is selected, due to the internal 1H delay inherent with this type of comb filter, the 1HL and 1HH signals are selected for the respective luma and chroma *SIMPLE* data signals. When any other type of comb filter is selected 0HL and 0HH are selected.

The DLYF selection bit is also internally generated from the type of comb filter selected and whether or not the input is in either the YC or Y & CbCr (ie D1 input) data formats. The *VIDEOB* data is always selected when the YCCOMP register bit is HIGH, ie for YC inputs. The selection of 1HF or 0HF depends upon the SIMP selection bit only when the YCCOMP register bit is LOW. Therefore, when YCCOMP is LOW and 0Hx is selected by SIMP then 0HF is selected for the *FLAT* signal, and when 1Hx is selected by SIMP then 1HF is selected for the *FLAT* signal. This ensures that the *FLAT* and *SIMPLE* data selected for any comb filter is delayed by the same amount as the data processed through the comb filter to produce the *COMB* output.

The final selection is the output required for the combed luminance and chrominance data. The output selection can be *SIMPLE*, *COMB*, *FLAT-COMB*, or *FLAT*. Generally *COMB* is selected based upon whether a luma or chroma comb was selected and the complementary output selects *FLAT-COMB*. In the YC and Y & CbCr data modes the *FLAT* signal selects the secondary data and *SIMPLE* or *COMB* can be used to select the primary signal. In these modes the bandsplit filter can be bypassed or used to remove low frequency noise from the chrominance signal if chroma was selected as the primary signal.

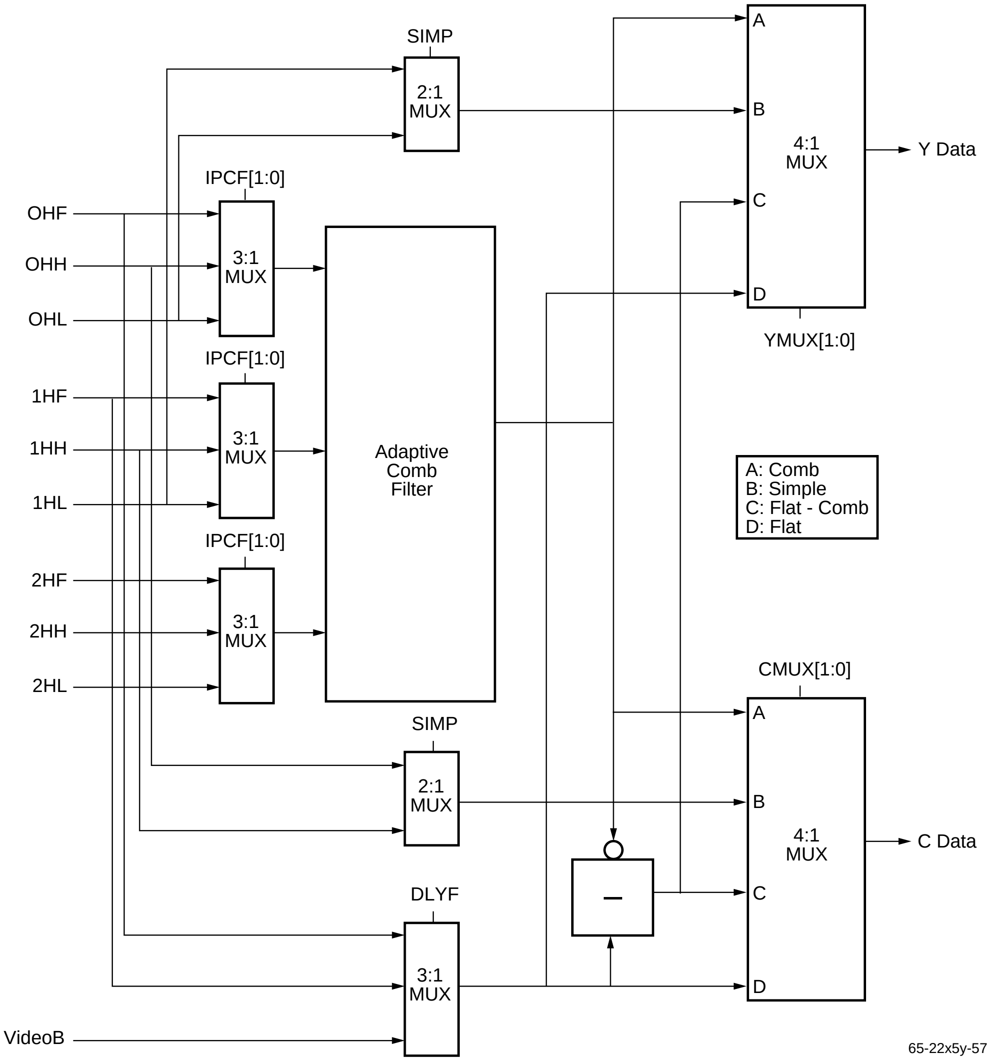


Figure 16. Signal Flow Around the Adaptive Comb Filter.

The comb filter architecture performs chrominance or luminance comb filtering on PAL or NTSC video signals, by implementing one of sixteen independent chroma and luma comb filter algorithms. The highest level of the adaptive comb filter configuration is determined by the STA[3:0] register bits as shown in Table 3.

Table 3. Comb Filter Architecture

STA[3:0]	Comb Filter Description
0	YC or Composite, PAL or NTSC, 3 line comb
1	YC or Composite, NTSC, 3 line comb (0H & 1H)
2	YC or Composite, NTSC, 3 line comb (1H & 2H)
3	YC or Composite, NTSC, 2 line comb (0H & 1H)
4	YC or Composite, NTSC, (2 line) field comb
5	YC or Composite, NTSC or PAL, field comb
6	YC or Composite, NTSC, (2 line) frame comb
7	YC or Composite, NTSC or PAL, frame comb
8	D1, Y or C_BC_R, 3 line comb
9	D1, Y or C_BC_R, 3 line comb (0H & 1H)
10	D1, Y or C_BC_R, 3 line comb (1H & 2H)
11	D1, Y or C_BC_R, 3 line comb (0H & 2H)
12	D1, Y or C_BC_R, (2 line) field comb
13	D1, Y or C_BC_R, field or 2 line comb (0H & 1H)
14	D1, Y or C_BC_R, (2 line) frame comb
15	D1, Y or C_BC_R, Frame

The *COMB* signal can be produced in two ways. The first method uses the comb fail detection circuits to select one of several comb filter architectures. These comb filter architectures weight the three lines by varying degrees depending upon the degree of picture correlation between the inputs to the comb filter. The simple example in Table 4 shows how this process works, in which upper denotes error comparisons between the two lines stores and lower denotes error comparisons between the input and the first line store. The 0H, 1H, and 2H terms used in the mathematical description of the comb filter selection refer to the position with respect to the internal line stores. The 0H term is the undelayed input, 1H is the output of line store 1, and 2H is the output of line store 2.

In this example a 3 line comb is implemented when in the flat areas of blue or yellow. However, when a difference between the inputs is detected the 3 line comb filter adapts to the 2 line comb filter whose inputs have the smallest difference. This illustrated on line n+4, at which time the comb filter adapts to inputs from 1H (blue) and 2H (blue) and ignores the 0H (yellow) inputs. In cases where there is a difference between all inputs to the comb filter, a 3 line comb filter is selected and the highest set of comb fail signals are sent to the XLUT input logic.

This technique would work well if pictures only contained vertical transitions, which is obviously not the case. Therefore the weighting of these comb filter taps, (0H, 1H, and 2H), are rarely just the simple ratios shown in Table 4. It is worth noting that comb filters that use an even number of lines in the comb filter architecture produce chrominance and luminance signals that are vertically offset by one picture line, i.e. in the middle of the even number of lines used in the comb filter input. While comb filters that use an odd number of lines, in the comb filter architecture, the chrominance and luminance produced is referenced to the center, i.e. the middle line, of the comb filter. This approach can consequentially cause aliasing in decoding composite video signals containing high frequency diagonal transitions. The FAST register bit, when set LOW, filters the comb filter selection to decrease the sensitivity of the adaption algorithm. The second method completely disables the adaption between different comb filters, by setting the ADAPT[1:0] register bits accordingly, see Table 5.

Table 4. Simple Example of an Adaptive Comb Filter Architecture

Line no.	Input color	Error signals						Comb filter selection
		upper luma	upper sat.	upper hue	lower luma	lower sat.	lower hue	
n+6	blue	x	x	x	x	x	x	unknown without line n+7
n+5	blue	0	0	0	0	0	0	[0H/4] + [1H/2] + [2H/4]
n+4	blue	0	0	0	>0	0	180	[0] + [1H/2] + [2H/2]
n+3	yellow	>0	0	180	0	0	0	[0H/2] + [1H/2] + [0]
n+2	yellow	0	0	0	0	0	0	[0H/4] + [1H/2] + [2H/4]
n+1	yellow	0	0	0	>0	>0	>0	[0] + [1H/2] + [2H/2]
n	black	x	x	x	x	x	x	unknown without line n-1

In either of these methods, the *"K"* signal can be used to cross fade between the *YCOMB* and the *SIMPLE* bandsplit signals. The resulting comb filter equation can be expressed as:

Combed Luma = Simple + (K * Combed High Frequency Luma)

Combed Chroma = Simple **-** (K * Combed High Frequency Luma)

In the case of the chroma comb, the weighted combed high frequency luma is subtracted from the *SIMPLE* high pass filter output to produce the combed chroma signal, and for luma comb filters the weighted combed high frequency luma is added to the *SIMPLE* low pass filter output to provide the combed luminance signal.

Comb Fails

The inputs to the comb filter are monitored to detect discontinuities that would cause the comb filter operation to fail. Whenever a significant failure is predicted, the comb filter architecture is modified and an error signal proportional to the discontinuity is produced. For flat areas of color, it is a relatively simple to produce an error signal that switches between the outputs of the comb filter and the simple band split filter without visibly softening the picture horizontally or vertically. However, as horizontal frequencies increase during vertical transitions, so the decision for switching between the comb and simple bandsplit decoder becomes more complex.

A line based comb filter can separate the luma and chroma signals from line repetitive composite video signals, with no loss of luma or chroma bandwidth. However, if there is a vertical transition, i.e. a change from one scan line to the next, as shown for a NTSC two line comb in Figure 17, a *comb fail* occurs. The comb fail shown in Figure 17, clearly illustrates the resulting vertical smearing of the luma and chroma signals.

In addition to the smearing, the resulting phase of the chrominance signal with respect to the burst can cause hue errors in the demodulated picture. In this example, the chrominance signal would be demodulated with a 180 degree phase error. Unlike the "simple" decoder technique any errors in the comb filter decoding produce components that if re-encoded will never reproduce the original composite video waveform. It is therefore imperative that the number and magnitude of comb fails be kept to its absolute minimum. This is not possible with non-adaptive comb filter architectures, and all vertical and diagonal transitions in the picture will cause irreversible picture degradation. For this reason, all the TMC22x5y comb filter decoders implement an adaptive comb filter architecture.

To aid in this decision making process, comprehensive comb fail signals are generated and fed to a user-programmable lookup table (XLUT). The output of the lookup table provides the control for the cross fade between the comb and simple bandsplit decoder.

Comb Fail Detection

The traditional approach of using the low frequency data to look for vertical luma transitions, and rectifying the high frequency data to estimate vertical transitions in the chroma provides adequate comb fail detection. However, chroma signals that are equal in magnitude but 180 degrees apart in phase, which can also have a small difference in luma level, for example green and magenta, can produce undetected comb fails in the comb filter output.

To overcome problems with simpler comb fail measurement techniques, the TMC22x5y generates an array of patented comb fail and comb filter control signals. To produce these signals each input to the comb filter is passed through a simple bandsplit decoder. This provides a luma signal from the low frequency portion of the comb filter input, and the hue (phase) and saturation (magnitude) from the high frequency portion of the comb filter input. These signals are compared and the differences in luma, hue, and saturation are used to determine the type of comb filter used to generate the *YCOMB* signal and to provide the cross fade control signal *"K"*. The *"K"* signal can be weighted within the XLUT lookup table, allowing the user to tailor the comb filter response to their system requirements.

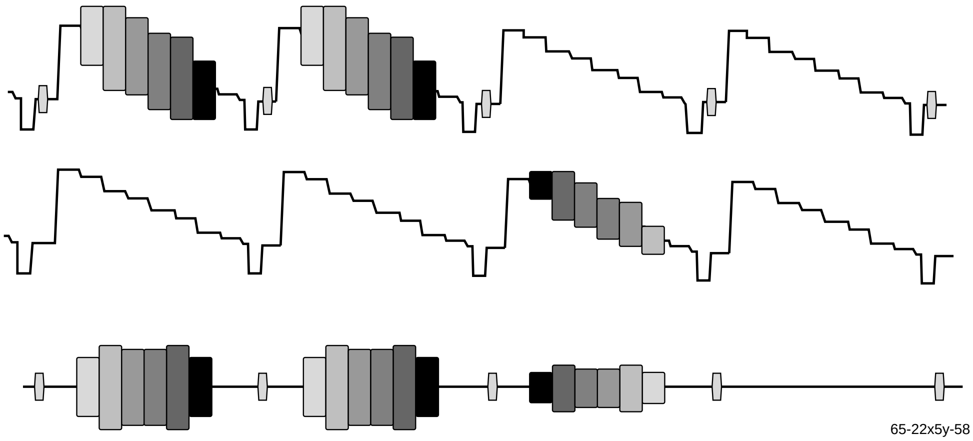


Figure 17. Example of a Comb Fail Using a NSTC Two Line Comb Filter

Generation of the Comb Fail Signals

Luma Error Signals

The signals from the 3 low pass filters, 0HL, 1HL, and 2HL are subtracted from one another to produce an error signal proportional to the luma comb fail. The resulting signals (0HL - 1HL), produces *LYE,* and either (1HL - 2HL) in NTSC or (0HL - 2HL) in PAL produces *UYE*. The *LYE* and *UYE* luma error signals are rectified if negative. In cases where the luminance component is constant, the error will be zero. Where the luminance goes from black to white over 2 lines, the error signal will go to its maximum value.

The luma error signals can be doubled to facilitate inputs with low picture levels by setting the YESG register bit HIGH. The resulting signal is clipped to ensure no overflow occurs

Hue and Saturation Error Signals

In the past, comb decoders have relied upon comparing the difference in chroma magnitude between two lines to determine a comb fail. In fact, this chroma signal is normally the output of the high-pass or band-pass filter, and therefore contains all the high frequency luminance information as well. As this signal was never demodulated, the sign bit was immaterial and was used only to rectify the chroma signal. This allowed chroma signals which where equal in magnitude but opposite in phase, and high frequency luminance signals, to fool the comb fail circuit.

The TMC22x5y uses a new, innovative approach to overcome this problem. To detect comb failures in the high-frequency portion of the video signal the outputs from the three high-pass filters, 0HH, 1HH, and 2HH, are passed through simple demodulators. The outputs from which provide the phase and magnitude of the in-phase and quadrature components of the high frequency data. These components are compared to determine the difference in phase and magnitude between 0H & 1H in all configurations, *LME* and *LPE*, and between 1H & 2H in NTSC or 0H & 2H in PAL, *UME* and *UPE*. The magnitude error signals can be doubled to facilitate inputs with low picture levels by setting the CESG register bit HIGH. The doubled magnitude error signals are limited to ensure no overflow occurs.

The algorithm used to separate the quadrature components depends upon the relationship between the normalized subcarrier frequency and the number of pixels per line. This algorithm is preset for either a NTSC/M or PAL/I subcarrier frequency and a pixel data rate of 13.5MHz. It is therefore necessary to compensate for other pixel data rates by selecting the appropriate default using the CEST[1:0] register bits.

Picture Correlation

The degree of picture correlation depends upon the differences between the *UYE, UME,* and *UPE* upper error signals and the *LYE*, *LME,* and *LPE* lower error signals, and is measured as a percentage of full scale error. In flat fields of color you would have 0% error in picture correlation, however in sharp vertical transitions say between yellow and blue you would have large % errors between *UYE* and *LYE* and between *UPE* and *LPE*, while there would be 0% error between *UME* and *LME*.

Adapting the Comb Filter

In NTSC it is possible to switch from a 3 line comb to a 2 line comb, and then to a simple decoder output. The 3 line comb to 2 line comb switch can be disabled, forcing the 3

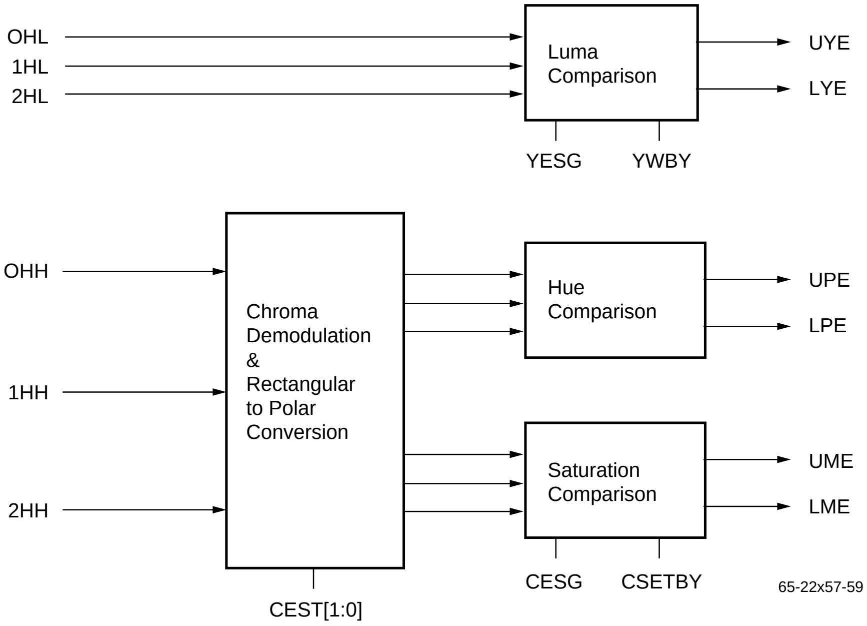


Figure 18. Generation of Upper and Lower Comb Fail Signals

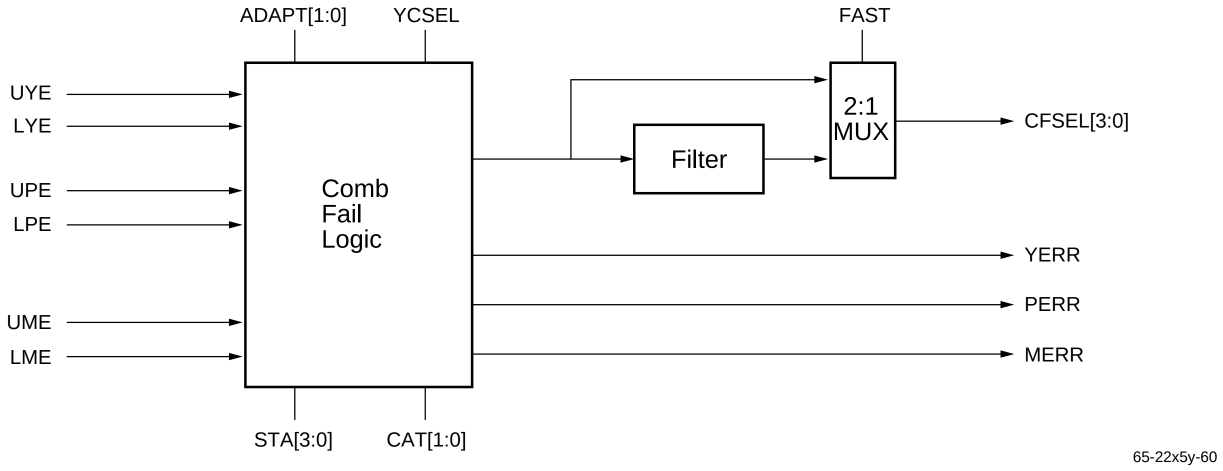


Figure 19. Comb Filter Selection

line comb to switch directly to simple. The switching between these two comb architectures is independent of the mix signal, K. For 3-line Y/C comb filters, an external 1H delay is required in the uncombed channel to compensate for the comb filter delay.

This principle is equally true for NTSC frame and field based comb decoders. The feature is not available for any of the PAL comb filter architectures.

The Comb filter Adaption Threshold register bits CAT[1:0] determine if 5%, 15%, 25%, or 50% errors in picture correlation is required to adapt the NTSC comb filter. In NTSC, due to the 180 degree advance in subcarrier phase per line, it is possible to switch between the 3 line comb and the choice of either the upper two line comb or the lower two line comb. If this switching occurs on a pixel by pixel basis the picture will contain vertical alias components. This artifact can be reduced by either setting the FAST register bit LOW, which filters the comb filter selection, and/ or setting the CAT[1:0] register bits to a higher percentage threshold.

The comb filter adaption is further controlled by the ADAPT[1:0] register bit selection, when the COMB[3:0] register bits select a 3 line comb. These bits control if the comb filter adapts from a 3 line comb to the best of the upper or lower 2 line combs, from a 3 line comb to just the lower 2 line comb, performs a fixed 3 line comb, or implements a best of two 3 line combs in PAL. If the COMB[3:0] register bits select one of the 2 line comb filters, the ADAPT[1:0] register bits are ignored, and no adaption is implemented. The CFSEL[1:0] signal, shown in Figure 19, controls which comb filter is selected on a pixel by pixel basis, and can be externally monitored by reading CFSTAT[1:0] in register 4Bh.

Table 5. Adaption Modes

ADAPT[1:0]	Function
00	Adapts to the best of 3 types of line based comb filters in NTSC only.
01	3 line (tap) comb always adapts to lower 2 line (tap) comb, when the 3 line (tap) comb fails. Normally used with NTSC field and frame based comb filters.
10	3 line (tap) comb only. Never adapts to a 2 line(tap) filter. The higher set of comb filter error signals are sent to the XLUT. NTSC or PAL comb filter.
11	Adapts to best of two 3 line comb filters in PAL only.

XLUT

The comb fail signals control both the comb filter adaption and the cross fade between the adaptive comb filter output *YCOMB* and the *SIMPLE* bandsplit signal. Which of the fail signals is fed to the XLUT is determined by which comb filter is selected in NTSC. When a 3 line comb filter is selected, the larger set of error signals are sent to the XLUT, when a upper 2 line comb is selected *UYE*, *UME*, and *UPE* error signals are selected, and when a lower two line comb filter is selected the *LYE*, *LME*, and *LPE* error signals are selected.

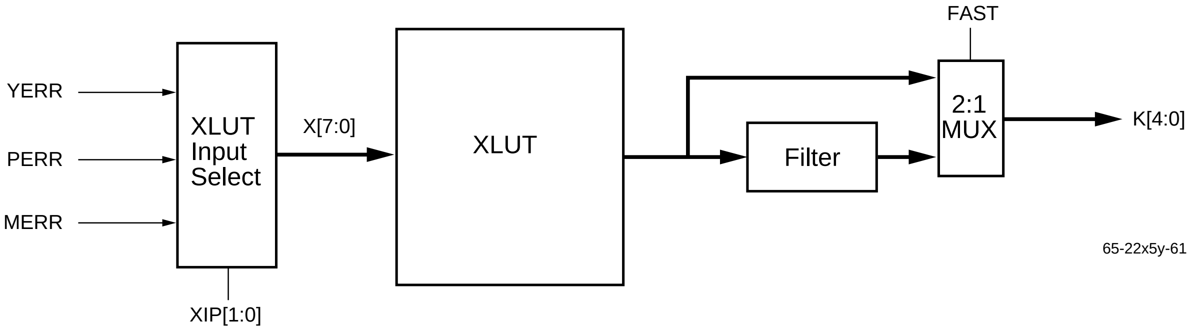


Figure 20. XLUT Input Selection

For PAL comb filters the *LYE*, *LME*, and *LPE* errors signals are always selected by default. In this way the error signals into the XLUT always represent the comb filter being implemented. The resolution of the error signals selected is controlled by the XIP[1:0] register bits as shown in Table 6: XLUT Input Selection. The position of these error signals on the XLUT input address X[7:0] is also shown.

Table 6. XLUT Input Selection

XIP[1:0]	Function
00	2 bits of phase error (X[7:6]), 3 bits of chroma (X[5:3]) and luma magnitude error (X[3:0]).
01	4 bits of chroma (X[7:4]) and luma magnitude error (X[3:0]).
10	3 bits of phase error (X[7:5]), 3 bits of chroma magnitude error (X[4:2]), and 2 bits of luma magnitude error (X[1:0]).
11	4 bits of phase error (X[7:4]) and chroma magnitude error (X[3:0]).

The selected comb fail signals are translated by the user-programmed configuration within the 256*5 XLUT into the mix signal (K) which controls the 30 levels of cross-fade between the weighted comb filter and the band split filters. The 1 to 31 mix signal is modified on the input to the cross-fade to produce a 0 to 32 control signal, as shown in Table 7.

Table 7. XLUT Output Function.

XLUT OUTPUT	K
0	Special function (e.g. luma comb and HPF on chroma)
1	0 - 100% Bandsplit
2	2
3	3
:	:
16	16 - 50% Bandsplit, 50% Comb
:	:
29	29
30	30
31	32 - 100% Comb

The special function assigned to K = 0 is programmed into the XSF[1:0] register bits, as shown in Table 8.

Table 8. XLUT Special Function Definitions

KIP_{1-0}	XLUT special function selection	
	Y	C
00	comb	simple
01	simple	comb
10	flat with notch	simple
11	flat with notch	comb

The “Flat with notch” selection passes the *FLAT* input through onto the luminance channel and selects the notch filter, centered at 0.25 of the normalized clock frequency. This mode is therefore only useful with inputs at 4*Fsc or in cases when a notch at 0.25 of the normalized clock frequency is adequate for application.

The XLUT output, is fed through a bypassable low-pass filter KLPF to avoid switching between comb and simple decoders on a pixel by pixel basis. When the special function is selected (K = 0) the input to the KLPF is held and the filter is automatically bypassed. The output of the XLUT can be externally monitored by reading XOP[4:0] in register 4Bh.

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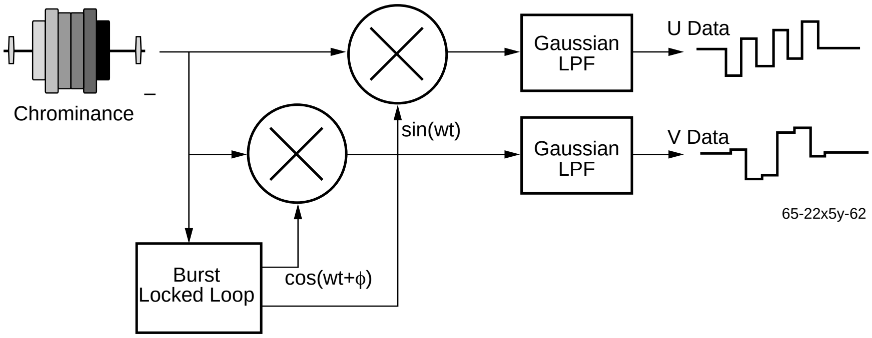

Figure 21. Block Diagram of Digital Burst Locked Loop

Digital Burst Locked Loop

The digital burst locked loop provides sine and cosine signals which are phase locked to the incoming burst signal. These sine and cosine signals are used to demodulate the chrominance data, producing the U and V color-difference signals. The U data are phase-referenced to sin(wt) and the V data to cos(wt). The demodulated signal is passed through a low pass filter to remove signals at twice the subcarrier frequency. The magnitude of the U and V data within the demodulated burst signal provides the error signal which, after filtering, is used to adjust the frequency and/or phase of the subcarrier DDS. The output of the subcarrier DDS is translated into sine and cosine signals in ROM-based lookup tables.
The PALODD signal is low on lines without the 180 degree phase advance in the modulated V signal, termed NTSC lines, and high for lines with the 180 degree phase advance, termed PAL lines. This signal is used in the burst locked loop to advance the phase of the cosine table on PAL lines. PALODD is always low for NTSC.

Color Kill Counter

The demodulated U and V components are compared to a programmable burst level threshold. If both the U and V data fall below this threshold, a color kill flag is set high. The color kill counter is incremented once per line if the color kill flag is high. If the count reaches 127 within one field, the color kill circuit becomes active during the next field group. When this occurs, the input video will be passed unaltered on the luminance channel and the color difference signals will be set to chroma black.

The color kill signal remains active until a field with less than 127 lines without burst is encountered, at which time, during the next vertical blanking period, the decoder is reset. The operation of the color kill logic can be monitored externally by reading the MONO register bit in register 44h. The MONO bit is HIGH for composite and YC video signals and LOW for monochrome signals.

Field Flag, FLD

The FLD signal is the lsb of the field count FID_{2-0} and is LOW for fields where the first vertical sync occurs in the first half of the line and is HIGH for fields when it occurs in the second half of the line. This signal is synchronized with the frame and color frame flags in the FID generator.

Frame Bit

NTSC
The middle bit (frame bit) of the field count is determined, by the phase of the subcarrier on a given pixel and on a given line. The signal used to determine this is NFDET (New Field DETect), and occurs when the line count is zero and the pixel count is one of four programmable pixel positions, zero, one, two, or three.

PAL
The frame bit in PAL is detected through the Bruch blanking sequence. The error signal control circuit generates a color kill flag whenever a line is detected without a burst. It is therefore possible to compare this signal with specific line idents to determine the field sequence in both PAL-I and PAL-M. A set of specific patterns determine the correct phase of FID_1; if any of these patterns is detected then FID_1 is forced to a known state and then flywheels until the next fixed pattern is detected.

Table 9. PAL-B,G,H,I Bruch Blanking Sequence

Internal line #	Burst present	Internal frame #	Internal field #
5	No	0 or 2	0 or 4
309	No	0 or 2	0 or 4
6	Yes	0 or 2	1 or 5
309	No	0 or 2	1 or 5
5	Yes	1 or 3	2 or 6
309	Yes	1 or 3	2 or 6
6	No	1 or 3	3 or 7
309	Yes	1 or 3	3 or 7

The frame bit is low for frames 0 and 2 and high for frames 1 and 3.

Table 10. PAL-M Bruch Blanking Sequence

Internal line #	Burst present	Internal frame #	Internal field #
7	No	0 or 2	0 or 4
258	Yes	0 or 2	0 or 4
7	No	0 or 2	1 or 5
259	No	0 or 2	1 or 5
7	Yes	1 or 3	2 or 6
258	No	1 or 3	2 or 6
7	Yes	1 or 3	3 or 7
259	Yes	1 or 3	3 or 7

The frame bit is low for frames 0 and 2 and high for frames 1 and 3.

PAL Color Frame Bit

The PAL color frame bit is the msb of the field count, FID_2. In NTSC this is always low, as NTSC has only a 4 field sequence. For both PAL-I and PAL-M inputs, the PAL color frame bit is determined in the same way the frame bit is determined in NTSC, by using the phase of the subcarrier on a given pixel and on a given line.

Hue Control

One of two programmable 16 bit system phase offsets can be added to the subcarrier oscillator between SAV and EAV. The selection is made by the BUFFER pin. This feature allows the user to change the picture hue on known frames without affecting the burst locked loop.

System Monitoring of the Burst Loop Error

The burst loop error signal is stored once per line in an 8 bit register that can be accessed over the microprocessor port. This allows the user to check for non-mathematical PAL inputs and to the change the decoder architecture from frame-based to line-based or simple decoder depending on this information.

Demodulation Low Pass Filter

There are two different demodulation low pass filters that can be selected under software. For PAL inputs with normalized subcarrier frequencies greater than 0.3 of the sampling frequency, it is recommended you use “demodulator filter 2” to stop aliasing of the second harmonic of the demodulation chrominance signal and the baseband color difference signals. Gaussian filters are used for both demodulation filters as they have no negative coefficients and therefore have no undershoots or overshoots which could cause in-band ringing.

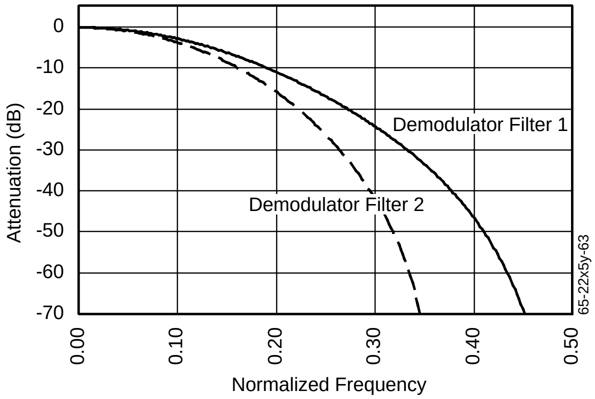

Figure 22. Gaussian Low Pass Filters

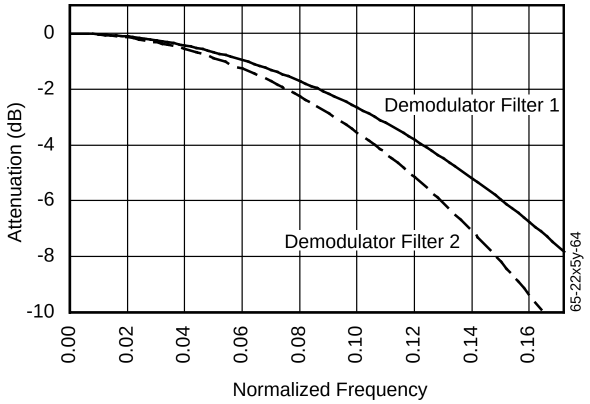

Figure 23. Gaussian LPF Passband Detail

Bypassing the Chrominance Demodulator

The demodulation of the chrominance signal needs to be bypassed when the decoder is processing C_BC_R component data or when a YC output is required. The bypass operation is controlled by the DMODBY register bit.

Bypassing the Demodulation Low Pass Filter

The demodulation low pass filter needs to be bypassed when processing C_BC_R component data or when a YC output is required. The C_BC_R data can also be passed through the Gaussian filter if the bandwidth needs to be reduced. The bypass operation is controlled by the GAUBY register bit.

Chrominance Coring

Chrominance coring, when active, sets the lsbs of the chroma channel (below a programmable threshold) to zero.

$VMCR_5$ Operation

When $VMCR_5$ is HIGH, the decoder will grab one line of video in LSTORE1. This effectively removes the comb filter from the decoding process, and the comb filter output is forced to simple mode.

Preliminary Information

Output Processor

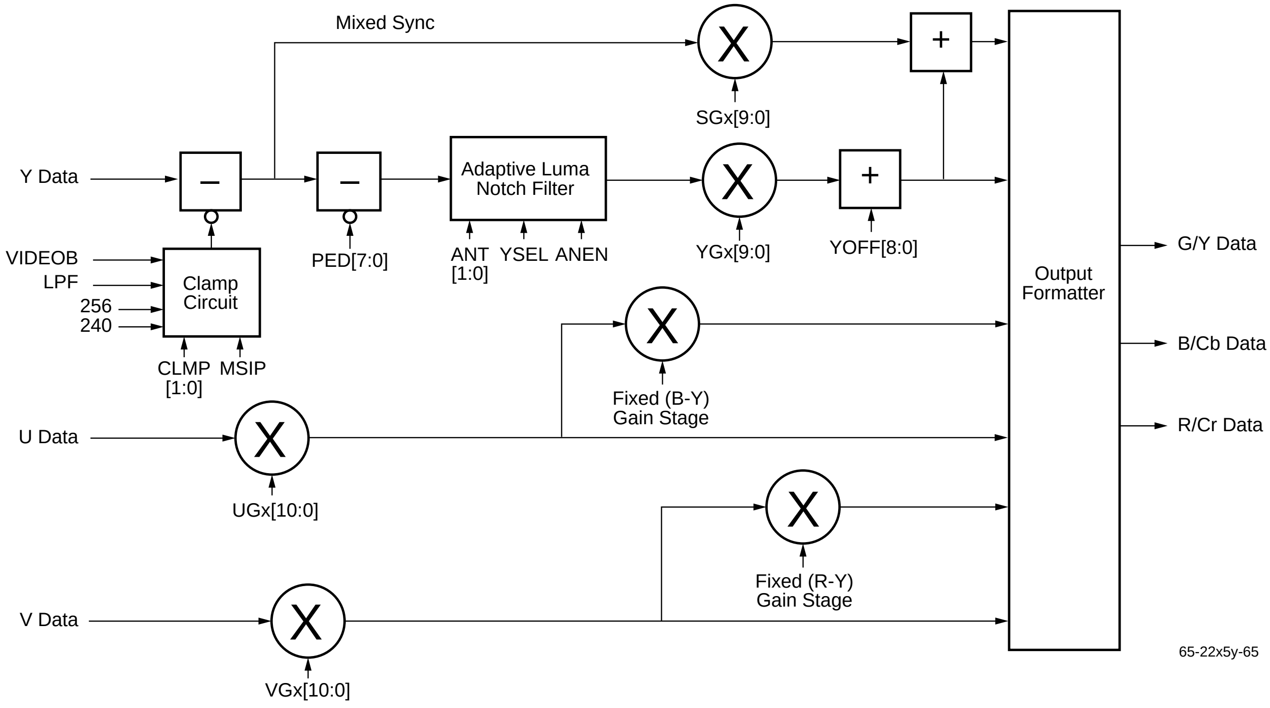

Figure 24. Output Processor Block Diagram

Clamp Circuit

A clamp pulse generated by the Burst Gate signal is used to grab either a sample of the low-pass-filtered luma during the video back porch, the signal on VIDEOB, or one of two internally generated levels. The selection is made by the CLMP[1:0] register bits.

Table 11. Blanking Level Selection

CLMP[1:0]	Blanking Selection
00	Internal 240 level
01	Internal 256 level
10	External VIDEOB Input
11	Internal LPF Output

The blanking level is subtracted from the decoded luma. If the sign is negative, the result is assumed to be mixed sync and is passed through a delay and into the sync gain stage within the output matrix. If the sign is positive, the result is assumed to be pure luma (blanking to peak white) and is fed to the pedestal removal circuit.

Pedestal Removal

The 8 bit programmable pedestal is subtracted from the pure luma signal. The negative super black signals are clipped to zero when register 0Ah bit 4 is set LOW, or the super black signals are passed through the luma scalar when register 0Ah bit 4 is HIGH.

Adaptive Notch Filter

The PAL line-locked comb decoder can never provide perfect subcarrier cancellation due to the 25Hz offset in the subcarrier frequency. This 25Hz offset causes residual and phase modified subcarrier to be left on the luminance signal which can produce a visible dot crawl on flat areas of color. However, for all comb filter structures, the quality of the comb depends on the quality of the sampling clock, as line to line clock jitter will also cause small phase changes between the inputs to the comb filter. It is therefore possible that NTSC comb decoders may also require some coring of the luma output. To meet the wide range of sample frequencies that the decoder must deal with two separate coring filters are selectable.

The luma signal from the pedestal stripper is compared against the preceding pixel to detect the magnitude change between pixels. This magnitude difference will be almost zero for flat areas of picture, and large for high frequency changes in the picture. The magnitude difference is compared to one of four programmable thresholds. The programmable threshold is selected by the ANT_{1-0} register bits as shown in Table 12.

Table 12. Adaptive Notch Threshold Control

ANT_{1-0}	Magnitude difference
00	less than 16
01	less than 12
10	less than 8
11	less than 4

If either of the error signals indicates that the magnitude difference is above the programmed threshold, or if ANEN is LOW, the adaptive notch filter is bypassed. The output of the adaptive notch filter is rounded to 8 or 10 bits, or the luma data that bypasses the coring filter is truncated to 8 or 10 bits depending upon the CORO register bit.

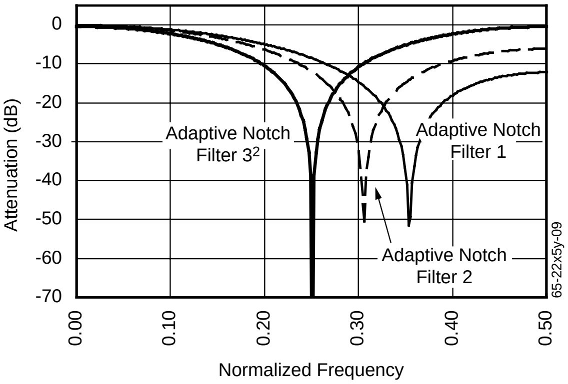

Figure 25. Adaptive Notch Filters

Luma Notch Filter

The simple luma notch filter is centered at 0.25 of normalized frequency, it therefore intended for use only in the subcarrier mode (4 * fSC) and for limited use with 13.5MHz NTSC as the subcarrier sits at 0.265 of normalized frequency. The notch filter is enabled by setting the NOTCH register bit HIGH.

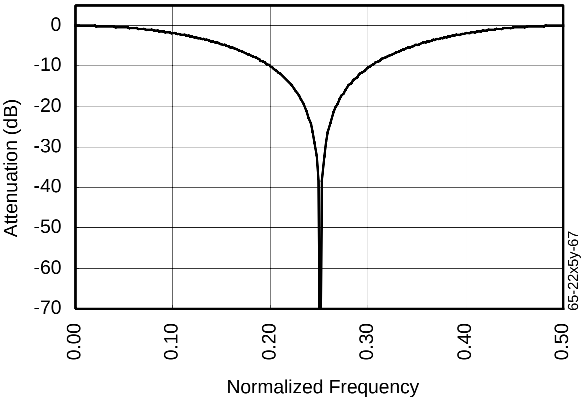

Figure 26. Luminance Notch Filter

Matrix

The magnitude of the decoded luminance and color difference signals will vary, not only with the standard, but also with the input mode. For this reason the output matrix contains programmable multipliers, and not just fixed scaling factors. The following sub sections explain the different scalar in the output matrix. The gain term in the Y, mixed sync, U and V scalar is the same - only the weighting makes them different. The scalar are capable of independently providing 6dB of gain if required.

Programmable U Scalar

The U scalar (UGx) provides the weighting required to produce (B-Y) or C_B from the demodulated U signal.

hence

(B-Y) = UGx * U

where UGx = gain / 0.493, and

C_B = UGx * U

where UGx = (gain * 448) / Umax

UGx has a scaling range of 0 to (2047/256).

Programmable V Scalar

The V scalar (VGx) provides the weighting required to produce (R-Y) or C_R from the demodulated V signal.

hence

(R-Y) = VGx * V

where VGx = gain / 0.877, and

C_R = VGx * V

where VGx = (gain * 448) / Vmax

VGx has a scaling range of 0 to (1023/256).

Programmable Y Scalar

The Y scalar (YGx) provides the scaling for the luminance signal if the output is YC_BC_R, or controls the magnitude of the RGB output along with the U scalar and V scalar. It is not possible to control the magnitude of the RGB signals independently.

YGx has a scaling range of 0 to (1023/256).

Programmable MS Scalar

The sync scalar (SGx) provides the scaling for the sync signal if the output requires sync on RGB. The programmed sync scaling factor is used during the horizontal and vertical burst blanking periods. During the active lines, the luma scaling factor is used to allow scaling of “super blacks” etc., which will be passed down the mixed sync path because they fall below the clamp level.

SGx has a scaling range of 0 to (1023/256).

Fixed (B-Y) and (R-Y) Scalars

These two scalars are zero when the output is YC_BC_R and provide the (B-Y) and (R-Y) weighting when the output is RGB. These are fixed scaling factors and are derived from the following equations.

(G-Y) = - [(0.299/0.587) * (R-Y)]
- [(0.114/0.587) * (B-Y)]

or

(G-Y) = - [(1043/2048) * (R-Y)]
- [(398/2048) * (B-Y)]

Preliminary Information

Y Offset

The 8 bit Y offset adds any offset required in the Y or RGB data outputs. For example 64 (16) for the 64 (16) to 940 (235) 10 bit (8 bit) 601 outputs. When the output is YC_BC_R this offset is applied to the luminance data only. The Y offset also provides the blanking level for RGB outputs with syncs.

Matrix Limiters

The different limiters are listed below, 10 bit data is assumed.

Table 13. Matrix Limiters

LMT$_{1-0}$	Comments
00	RGB output format, limited from 0 to 1023
01	YC_BC_R output format, Y limited from 0 to 1023 and C_BC_R limited to +/- 511.
10	RGB output format, limited from 64 to 940
11	YC_BC_R output format, Y limited from 64 to 940 and C_BC_R limited to +/- 448

Examples of Output Matrix Operation

From the SMPTE-170M specification:

Color	Y	U	V
White	584	0	0
Yellow	523	-236	54
Cyan	423	79	-332
Green	361	-156	-278
Magenta	267	156	278
Red	205	-79	332
Blue	105	236	-54
Black	44	0	0

YC_BC_R data ranges are:

Y data range is 64 to 940 (876)
C_BC_R data ranges are 64 to 960 (+/- 448)

Matrix programming:

YGx = (876 / 540) = 1 + (159/256)
UGx = (448 / 236) = 1 + (230/256)
VGx = (448 / 332) = 1 + (89/256)
YOFF = 64
PED = 44

Color	Decoder Output			CCIR 601 Spec		
	Y	C_B	C_R	Y	C_B	C_R
White	939	0	0	940	0	0
Yellow	841	-448	73	840	-448	72
Cyan	678	150	-447	678	151	-448
Green	578	-296	-376	578	-296	-375
Magenta	426	296	376	426	296	375
Red	325	-150	447	326	-151	448
Blue	163	448	-73	164	448	-72
Black	64	0	0	64	0	0

PAL digital composite input and RGB (0-1023) outputs:

Color	Y	U	V
White	572	0	0
Yellow	507	-250	57
Cyan	401	84	-352
Green	336	-165	-295
Magenta	236	165	295
Red	171	-84	352
Blue	65	250	-57
Black	0	0	0

The nominal scaling factors are simply:

YGx = 1023/572 = 1 + (202/256)
UGx = (1023/572)*(1/0.492) = 3 + (163/256)
VGx = (1023/572)*(1/0.877) = 2 + (10/256)
YOFF= 0
PED = 0

Color	G	R	B
White	1023	1023	1023
Yellow	1023	1023	0
Cyan	1023	0	1023
Green	1023	0	1
Magenta	0	1023	1022
Red	0	1023	1
Blue	0	0	1023
Black	0	0	0

It is also possible with the architecture supplied to use the limiters on the output of the matrix to clip the output video deliberately by using a slightly larger gain than is required. The Y_Offset can achieve the same by setting its value to be one lsb less than the minimum clip level.

Buffer Registers

The BUFFER pin allows the user to externally switch between two sets of internal registers that have the same function. This register buffering allows the matrix gain, picture hue, and luma offset to be changed at a known time relative to the input data.

Registers 17 to 1D are selected when the BUFFER pin is LOW and registers 27 to 2D are selected when the BUFFER pin is HIGH. If the msb of the decoder product code DPC$_2$ is LOW, an 8 bit decoder has been selected and the bottom 2 bits of registers 17 to 1A and 27 to 2A are forced to zero.

Simple Luma Color Correction

If the YBAL register bit is set HIGH, and the luma data reaches or exceeds the luma limits, there should be no C_BC_R or UV data at that time; therefore the color data are set to ZERO. If YBAL is set LOW then the C_BC_R/UV data are unaffected by the luma data.

C_BC_R MSB Inversion

The msb of the C_BC_R data can be inverted by setting the MSBO register bit HIGH. As this would affect the chroma blanking level, this circuit appears at the output of the MATRIX circuit.

Output Rounding

For compatibility with 8 bit systems, the output of the matrix can be rounded to 8 bits by setting the RND8 register bit HIGH.

Output Formats

RGB Outputs

The RGB data are simply passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the green data path only.

YUV Outputs

The YUV data are simply passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the luminance data path only.

YC_BC_R Outputs

The YC_BC_R data can be output in 3 ways, depending upon the CDEC, F422, and YUVT register bits. These output modes are summarized in .

When CDEC is HIGH and F422 is HIGH, the G/Y output is set to 64 and the B/U output is set to 512 between the EAV TRS data word and the first preamble word of the SAV TRS, i.e. during the digital horizontal blanking period. When YUVT is HIGH, R/V is set to 512, 64, 512, 64, etc., starting after the EAV TRS data word and finishing before the SAV preamble.

Decimating C_BC_R Data

Whenever the CDEC register bit is set HIGH the B/U and R/V data are simply sample dropped, with respect to CBSEL, to produce the multiplexed C_BC_R data stream at the PCK clock rate. If the input was initially D1 then the dropped samples will be the interpolated samples produced by the chroma interpolation filter. If however the C_BC_R data are simply weighted UV data then the sample dropped demodulated color difference signals (UV) will alias around 0.25 of the normalized sample frequency.

Multiplexed YC_BC_R Output (TRS Words Inserted)

When both the CDEC and YUVT register bits are HIGH the Y, C_B, and C_R component data are multiplexed into a single 27MHz (PXCK) data stream with embedded TRS words. The TRS words are generated based on the $\overline{\text{HSYNC}}$ or $\overline{\text{VSYNC}}$ pulses provided to the decoder, and the internally derived horizontal blanking ($\overline{\text{HBLK}}$), vertical blanking ($\overline{\text{VBLK}}$), and the field flag (FLD). This mode of operation is only available if a line locked PXCK clock, at 27MHz, is provided. The TRS words will be generated with respect to the HSYNC\ signal as per the ANSI/SMPTE 125M-1992 and CCIR 656 specifications.

YC Outputs

The YC data are passed through to the decoder output. When the DRSEN register bit is HIGH the DRS data are inserted into the luminance data path only. The luminance appears on G/Y, chrominance is on B/U and the R/V output is set to zero, by setting the V_scalar to zero.

The LDV Clock

The decoder can accept clocks at either the pixel clock rate (PCK) or at twice the pixel clock rate (PXCK). In the cases where the clock provided is PXCK, for example the genlock mode, the output data still needs to be at the PCK clock rate. To aid in the design of external circuitry a LDV clock is provided if the LDVIO register bit is LOW, if LDVIO is HIGH then the LDV pin becomes an input for an external clock.

If an external LDV clock is employed the user must ensure that the rising edge of the external LDV meets the specified setup and hold times relative to the input CLOCK pin. The selection of which clock to use on the decoder output is set by the OPSEL register bit. When OPSEL is set LOW the output is clocked at the same rate as the clock on the CLOCK pin, and when OPSEL is set HIGH the output is clocked by the internal or external clock on the LDV pin.

Table 14. Output Format

CDEC	YUVT	F422	G/Y	B/U	R/V	Comments
0	x	x	G or Y	B or C_B	R or C_R	[4:4:4] data
1	0	0	Y	C_B	C_R	[4:2:2] data
1	0	1	Y	C_BC_R	0	[4:2:2] data
1	1	x	Y	C_BC_R	D1 data	[4:2:2] data & D1 output

Sync Pulse Generator

The vertical and horizontal references to the decoder can be from external VSYNC and HSYNC pulses, decoded from TRS and TRS-ID words, or from the internal sync separator which extracts the sync information from the digitized input video.

The sync pulse generator (SPG) provides all the clock and enable pulses required to synchronize the decoder operation to the incoming video signal. These pulses are described below, along with the microprocessor data required to control them.

Internal Field and Line Numbering Scheme

The internal line numbering of the digital decoder differs from the standard video line numbering as shown in the following tables. The internal line numbers for a 3 line comb advance the numbering by 1 line with respect to the input, but are identical with respect to the internally one line delayed decoded video.

Table 15. NTSC Field and Line Numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 3	1 - 3	1 & 3	260 - 262
1 & 3	4 - 263	0 & 2	0 - 259
2 & 4	264 - 265	0 & 2	260 - 261
2 & 4	266 - 525	1 & 3	0 - 259

Table 16. PAL B,G,H,I Field and Line Numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 5	1 - 312	0 & 4	0 - 311
2 & 6	313 - 625	1 & 5	0 - 312
3 & 7	626 - 937	2 & 6	0 - 311
4 & 8	938 - 1250	3 & 7	0 - 312

Table 17. PAL M Field and Line Numbering

Standard Field #	Standard Line #	Internal Field #	Internal Line #
1 & 5	1 - 262	0 & 2	0 - 261
2 & 6	263 - 525	1 & 3	0 - 262
3 & 7	1 - 262	0 & 2	0 - 261
4 & 8	263 - 525	1 & 3	0 - 262

HSTBG (Burst gate)[*]

The burst gate starts the 16 clock period average of the demodulated burst envelope. The position of the burst gate is programmed into a register as the number of clock periods from the falling edge of sync to the burst envelope.

$\overline{\text{HBLK}}$ (Horizontal Blanking Period)[*]

The horizontal blanking period is LOW between the start of SAV and the end of EAV. This signal is used in several places:

a) To clear the SYSPH offset when LOW, this is required for correct operation of the subcarrier phase locked loop,
b) To aid in the comb filter management,
c) To remove the burst envelope on the demodulated UV data,
d) To remove the syncs on the BLUE and RED outputs.

$\overline{\text{BBLK}}$ (Vertical Burst Blanking Period)

The vertical burst blanking blanks the lines with no burst from the burst phase locked loop. This signal is decoded from the line ident, LID$_{4-0}$, and is modified by the video standard and the field count.

$\overline{\text{MBLK}}$ (Mixed Blanking)

This signal is used in the matrix to switch between the sync scalar and the luma scalar. The $\overline{\text{MBLK}}$ signal is active whenever $\overline{\text{HBLK}}$ is active or becomes active when $\overline{\text{VBLK}}$ becomes active. $\overline{\text{MBLK}}$ is also active in PAL on line 310 when both VACT1 and FLD are HIGH and in NTSC and PAL M on line 259 when VACT2 is HIGH and FLD is LOW.

FLD[*]

The FLD is LOW for field 1 and HIGH for field 2.

LID$_{4-0}$[*]

The line ID signals are used in the vertical comb filter management to control the comb filter on the leading and trailing lines of active video around the vertical blanking period, to start and stop the VINDO operation, and in generating the vertical blanking and burst blanking periods.

VACT2[*]

VACT2 is HIGH during the second half of all active lines.

GRABF[*]

The GRABF signal goes HIGH when the internal field count is equal to the programmed field number for the GRAB operation. f a pixel grab is being, this signal is held HIGH to not inhibit the GRABS signal on each line.

GRABL[*]

The GRABL signal goes HIGH when the internal line count is equal to the programmed line number for the GRAB operation. If a pixel grab is being performed, this signal is held HIGH to not inhibit the GRABS signal on each line.

GRABP[*]

The GRABP signal goes HIGH when the internal pixel count is equal to the programmed pixel number for the GRAB operation.

$\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$ (Output Pins)

The $\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$ signals are active when GCR$_2$ is LOW. When GCR$_2$ is HIGH these signals are three stated. Three line comb based decoders have an inherent line delay, therefore the input $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ signals can not be just delayed by a few registers and output as $\overline{\text{DVSYNC}}$ and $\overline{\text{DHSYNC}}$: they need to be delayed by one complete line. In all other comb filter configurations the $\overline{\text{DVSYNC}}$ and

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[*] Signal is available over the microprocessor data bus.

$\overline{\text{DHSYNC}}$ are referenced to the input data (0HFLAT) and not the output of the LSTORE1, i.e. 1HFLAT.

The duration of the $\overline{\text{DVSYNC}}$ signal is fixed to one line and the duration of the $\overline{\text{DHSYNC}}$ signal is 64 clock periods. Both these signals are generated by the internal horizontal and vertical state machines.

The falling edge of these signals relative to the data matches the requirements of the TMC22x91 family of digital encoders.

AVOUT Active Video (Output Pin)

The decoder produces an active video signal starting 4 PCK before the programmed start of active video and ending 4 PCK after the programmed end of active video. This signal is used in both the video mixer (TMC22x8x) family and the digital encoder (TMC22x9x) family. The end points of this signal are flagged by the internally generated SAV and EAV signals.

$\overline{\text{VBLK}}$ (Vertical Blanking Period)**

The vertical blanking period conforms to the CCIR 656 specification for D1 component data streams. This signal is decoded from the line ident, LID_{4-0}, and is active low.

Table 18. Vertical Blanking Period

	Internal field no	Internal line no
NTSC	0,2	0 - 5
		260 & 261
	1,3	0 - 6
		260 - 262
PAL	0, 2, 4, & 6	0 - 21
		310 & 311
	1, 3, 5, & 7	0 - 22
		311 & 312
PAL-M	0, 2, 4, & 6	0 - 5
		260 & 261
	1, 3, 5, & 7	0 - 6
		260 & 262

$\overline{\text{BBLK}}$ (Vertical Burst Blanking Period)

The vertical burst blanking blanks the lines with no burst from the burst phase locked loop. This signal is controlled by the video standard and the field count. The burst blanking signal is active low.

Table 19. Vertical Burst Blanking Period

	Internal field no	Internal line no
NTSC	0,2	0 - 5
		259 - 261
	1,3	0 - 6
		260 - 262
PAL	0 & 4	0 - 5
		309 - 311
	1 & 5	0 - 5
		309 - 312
	2 & 6	0 - 4
		310 & 311
	3 & 7	0 - 6
		310 - 312
PAL-M	0 & 4	0 - 7
		259 - 261
	1 & 5	0 - 7
		259 - 262
	2 & 6	0 - 6
		258 & 261
	3 & 7	0 - 6
		260 - 262

LID_{4-0} List of Line Idents

The line numbers required to produce all the decoder control signals are summarized in

Table 20. Table of Line Idents, LID[4:0]

Line no:	LID_{4-0}
0	00
1 - 4	01
5	02
6	03
7	04
8	05
9 - 16	06
17	07
18	08
19 - 21	09
22	0A
23	0B
24	0C
25 - 257	0D
258	0E
259	0F

Preliminary Information

** Signal is available over the microprocessor data bus.

Table 20. Table of Line Idents, LID[4:0] (cont.)

Line no:	LID_{4-0}
260 & 261	10
262	11
263 - 307	12
308	13
309	14
310	15
311	16
312	17

Timing Parameters

Subcarrier Programming

The color subcarrier is produced by an internal 28 bit Direct Digital Synthesizer (DDS) which is phase locked to the burst signal of the digitized video input. The nominal frequency is programmed into the DDS as follows:

FREQ = (number of subcarrier cycles per line / number of pixels per line) * 2^28

An example would be NTSC subcarrier mode

FREQ = (227.5 / 910) * 2^28 = 4000000 hex

Horizontal Timing

The horizontal video line is broken down into four horizontal timing parameters.

STS: The number of pixels between sync pulses

STB: The number of pixels between the nominal mid point of sync and the start of the 16 pixel burst gate. This value is modified depending upon the mode of operation.

Table 21. Timing Offsets

Standard	Mode	Offset required
x	Genlock	-8
x	Line locked	-8
x	Subcarrier	-22
PAL	D2 mode	-12
NTSC	D2 mode	-8
x	D1 mode	+12

BTV: The number of pixels between the start of the 16 pixel burst gate and the nominal start of active video.

AV: The number of active pixels in the active video line.

The difference between the sum of STB+BTV+AV subtracted from STS provides the nominal front porch.

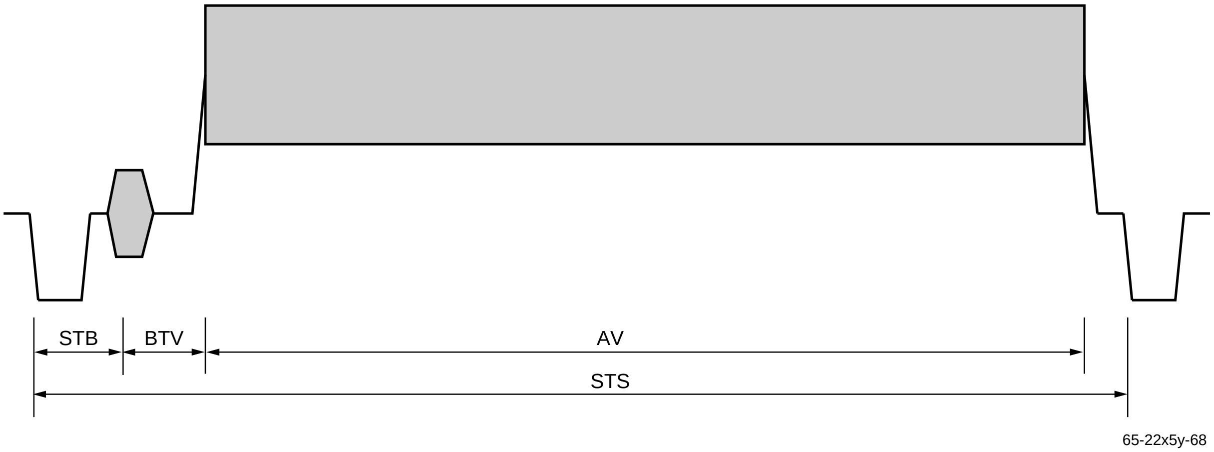


Figure 27. Horizontal Timing

Vertical Blanking

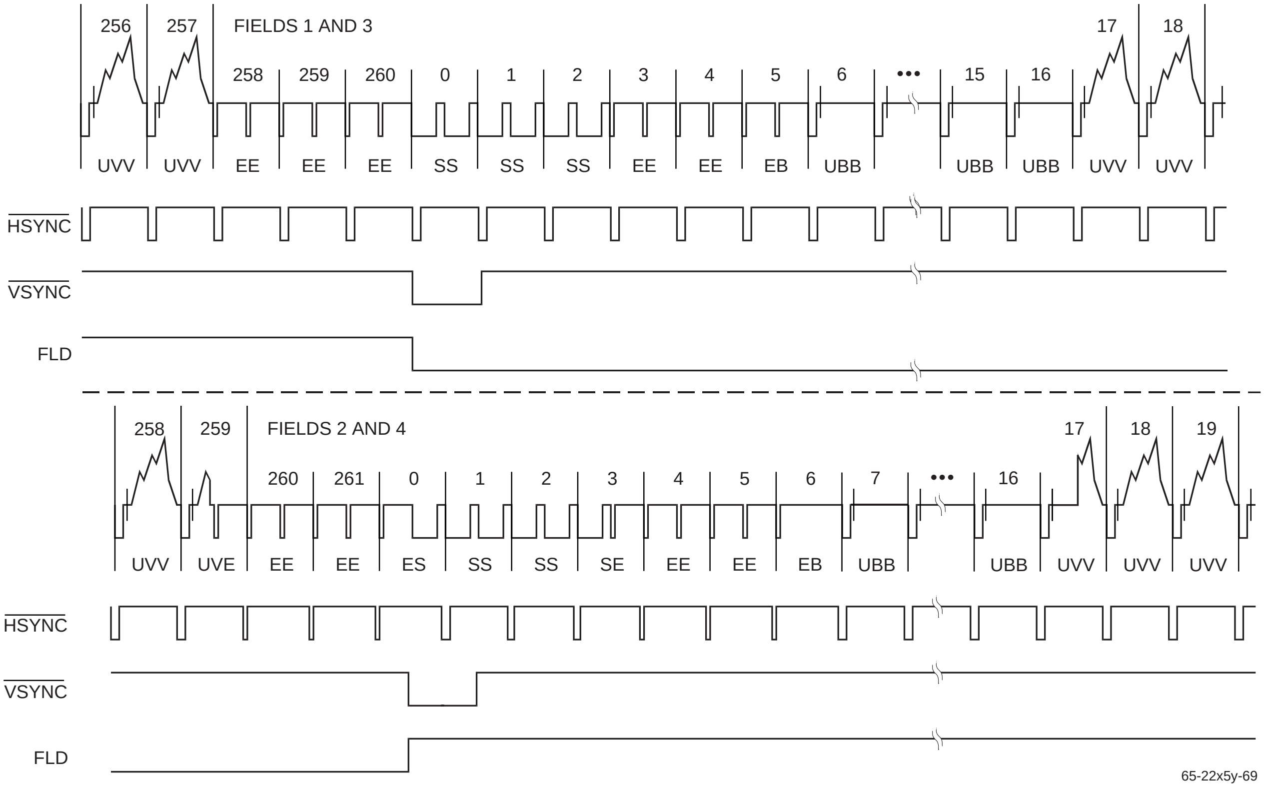


Figure 28. NTSC Vertical Interval

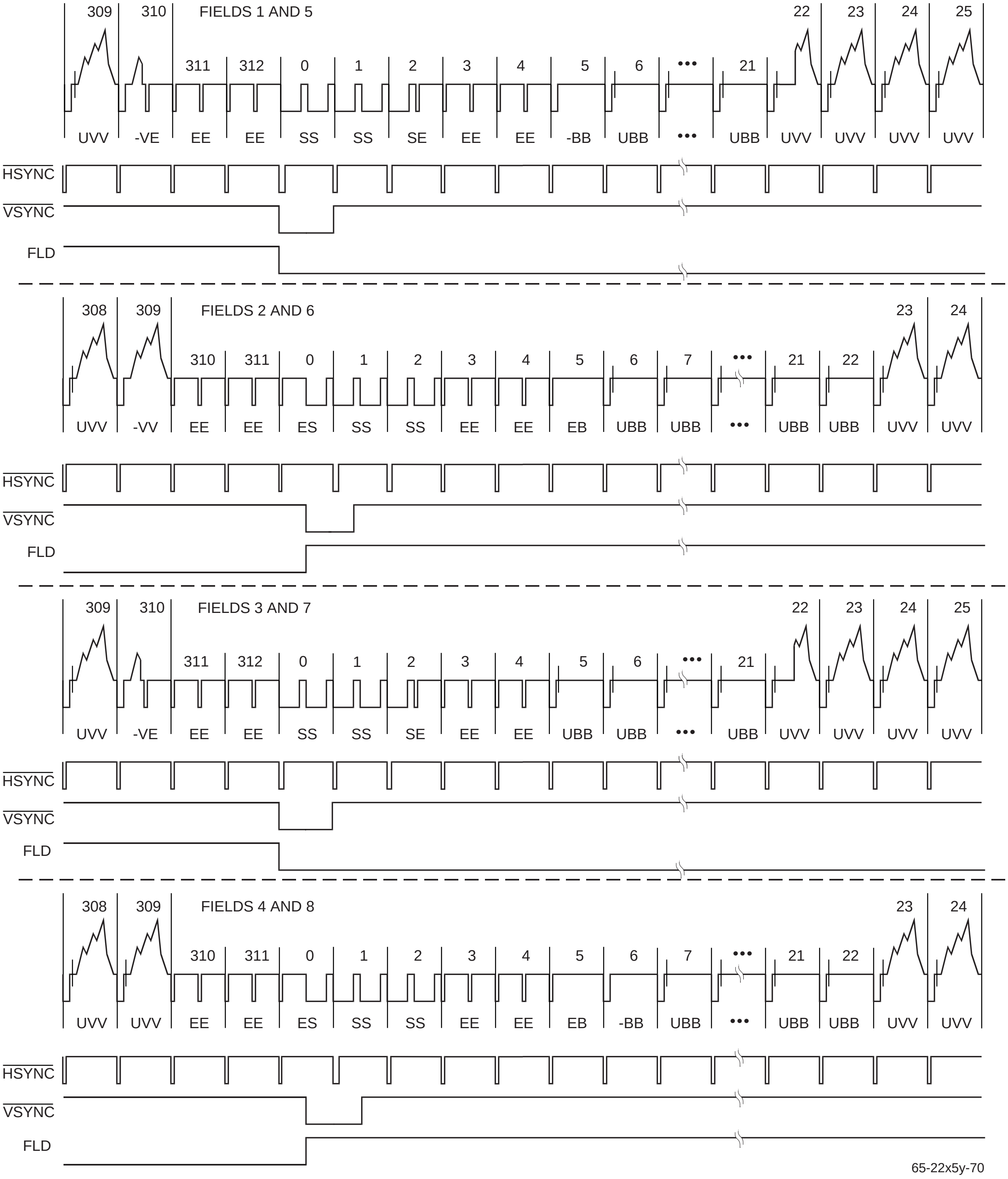


Figure 29. PAL-B,G,H,I,N Vertical Interval

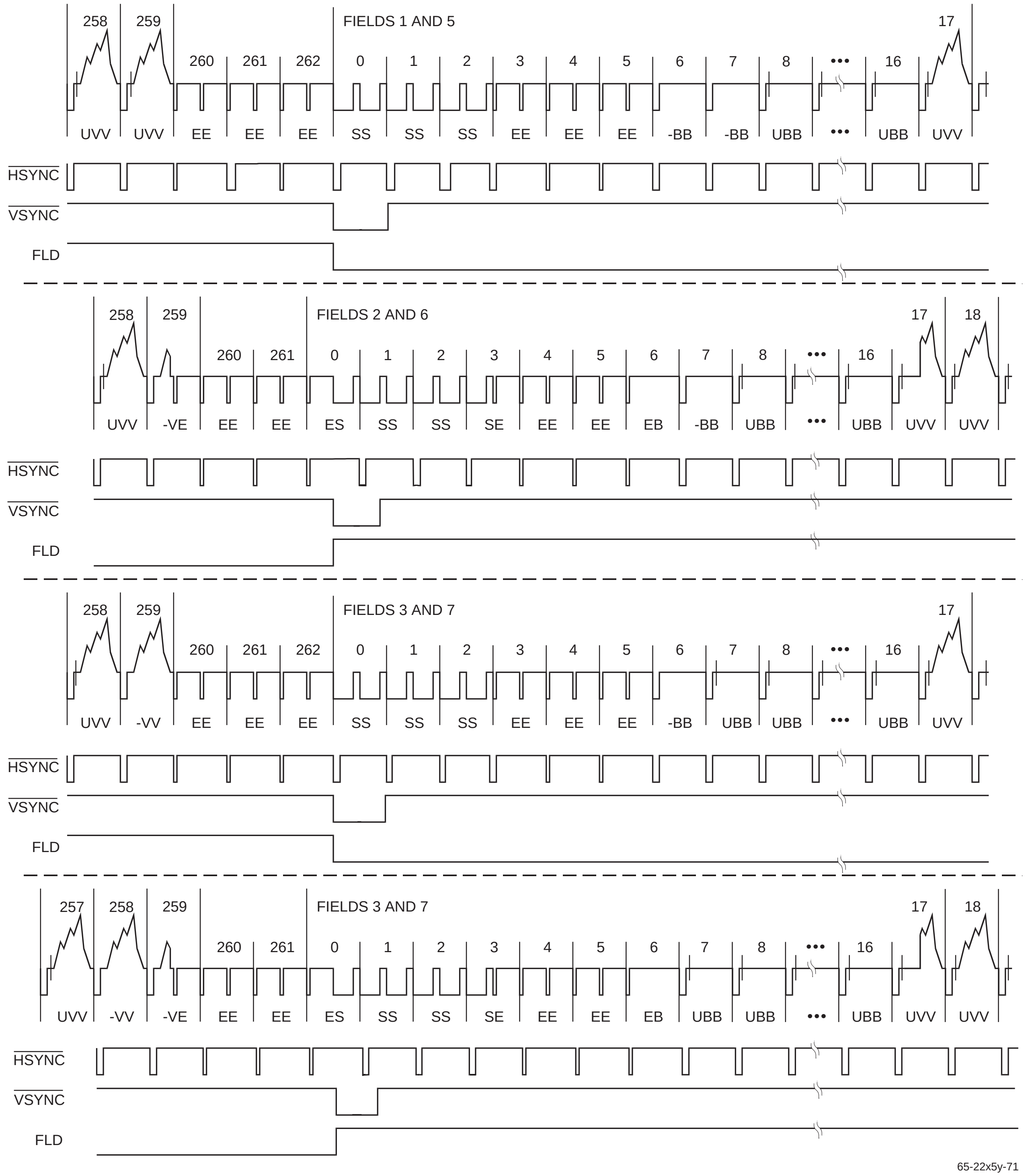


Figure 30. PAL-M Vertical Interval

VINDO Operation

The VINDO circuit uses the line idents on LID$_{4-0}$, and the blanking signals to control the comb filter output and the blanking of the YUV data in the output matrix during the vertical blanking period.

The vertical window VINDO starts on the first line after the last equalizing pulse, at LID$_{4-0}$ = 02. The VINDO stays HIGH from this line until the VINDO count = VINDO$_{4-0}$, or the $\overline{\text{VBLK}}$ signal goes HIGH, at which time the VINDO goes LOW. While the VINDO is HIGH the decoder operation is controlled by VDIV, and during the time the VINDO and $\overline{\text{VBLK}}$ are LOW the decoder operation is controlled by VDOV.

Table 22. PAL VINDO operation

LID$_{4-0}$	VINDO	VDIV	VDOV	Y	C
00 - 01	x	x	x	normal	normal
02 - 0A	1	0	x	simple	simple
02 - 0A	1	1	x	flat	black
02 - 0A	0	x	0	black	black
02 - 0A	0	x	1	simple	black
0B - 17	x	x	x	normal	normal

NTSC VINDO operation

LID$_{4-0}$	VINDO	VDIV	VDOV	Y	C
00 - 02	x	x	x	normal	normal
03 - 06	1	0	x	simple	simple
03 - 06	1	1	x	flat	black
03 - 06	0	x	0	black	black
03 - 06	0	x	1	simple	black
07 - 17	x	x	x	normal	normal

Video Measurement

The TMC22x5y supports a comprehensive set of video measurement techniques to aid the user in setting up the gain, phase, etc. of the decoder and in tracking down system errors.

Pixel Grab

The pixel grab allows the user to grab one pixel every line, or one pixel out of the four field sequence in NTSC or the 8 field sequence in PAL, under software control. The SET pin can also be used to produce the pixel grab pulse if SET$_{2-0}$ = 110 and PGEXT is set HIGH.

The 10 bit G/Y, B/U, R/V outputs are stored in one set of four 8 bit registers in the FORMAT block, while the 10 bit luma and mixed sync data and the 10 bit demodulated U and V color difference signals are stored in a set of five 8 bit registers in the GRAB circuit block. The pixel grab signal, PIXEL, whether internally or externally generated, is internally delayed to ensure that the all the grabbed data are from the same pixel relative to the line sync pulse. The PIXEL signal is equal to PGRAB or the logical AND of PGRAB with FGRAB and LGRAB, and is controlled by the LPGEN, PGEN, and PGEXT register bits.

The luma and mixed sync signals are multiplexed on the YMS data bus and the U and V signals are multiplexed on the UV data bus, at the PXCK clock rate. The pixel grab signal accommodates for this when grabbing these components.

An example of the pixel grab feature, is grabbing a pixel in the center of the burst period allowing the user to check the burst height by reading the magnitude of the demodulated U and V components. This allows the user to compensate for any chrominance gain errors in the output matrix.

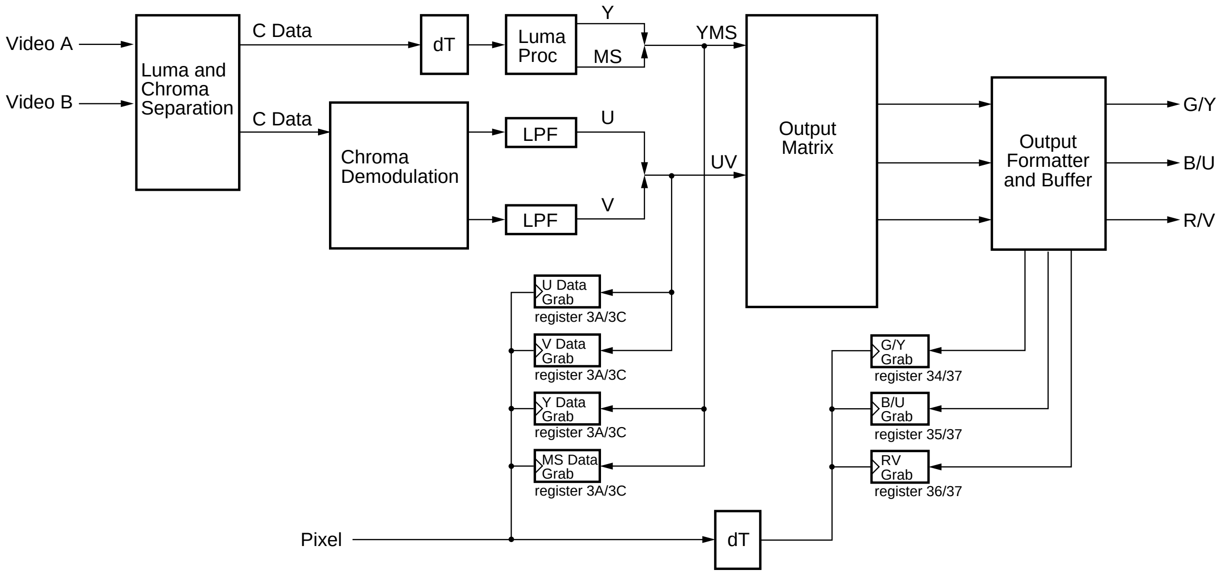


Figure 31. Pixel Grab Locations

Table 23. Pixel Grab Control

LGEXT	PGEN	PGEXT	LGEN	GRABS signal
0	0	x	x	GRABS = 0
0	1	0	0	GRABS = PGRAB
0	1	0	1	GRABS = FGRAB & LGRAB & PGRAB
0	1	1	x	GRABS = NOT (SET pin)
1	x	0	x	GRABS = PGRAB
1	x	1	x	GRABS = NOT (SET pin)

If a single pixel every 4 fields in NTSC and 8 fields in PAL is required to be grabbed, PGG and PGEN in register 30h should be set HIGH. The pixel grab signal is the logical AND of the GRABP, GRABL, and GRABF signals. GRABP goes HIGH whenever the pixel count equals the programmed pixel grab number, GRABL goes HIGH for one line whenever the line count equals the programmed line number, and the GRABF goes HIGH for a field whenever the field number equals the programmed field count.

If the same pixel on every line is required to be grabbed, then PGG should be set LOW, which internally forces GRABL and GRABF to be forced HIGH enabling the pixel grab whenever GRABP goes HIGH.

The SET pin can be used to provide an external grab signal when PGEXT is set HIGH in register 30h and the SET function in register 00h, SET[2:0] is programmed to 110 (binary). In this mode the falling edge on the SET pin triggers the pixel grab.

The GRABP, GRABL, and GRABF signals are available on bits 0,1, and 2 respectively of the read only register 41. An example of the pixel grab feature, would be grabbing a pixel in the center of the burst period allowing the user to check the burst height by reading the magnitude of the demodulated U and V components. This would then allow the user to compensate for any chrominance gain errors in the output matrix.

The pixel grab value is delayed by 28 pixels from the pixel count. This is the delay for all the pixel grab registers. Figure 32 shows this delay relative to GHSYNC. This means that if 28 is placed in the PG value, the actual pixel grabbed is pixel 0.

The top two bits of the PG value provide the quadrant and the bottom 9 bits provide the offset within that quadrant. The integer part of STS/4 gives the maximum count for each quadrant while the fractional result (bottom two bits) provides the 0,1,2, or 3 count offset for the last quadrant.

For pixels value <= 4*Int(STS/4)
PG[10:9] = quadrant number
PG[8:0] = max quadrant count - Int(STS/4) + pixel offset

For pixels value > 4*Int(STS/4)
The quadrant is always number 3, ie PG[10:9] = 11 while the pixel in excess of 4*Int(STS/4) is added to 1536.

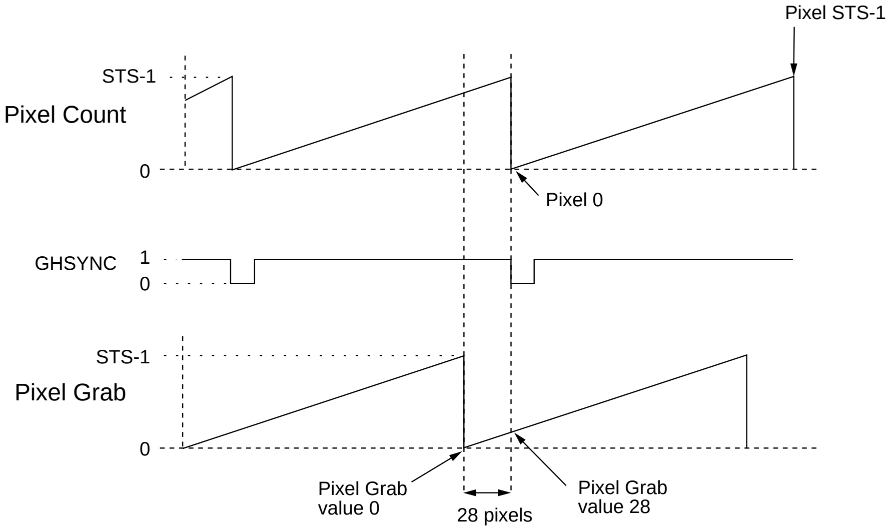


Figure 32: Relationship Between Pixel Count and Pixel Grab Value

Examples:

NTSC std with STS programmed to 858.
Base pixels per quadrant = Int(858/4) = 214

Pixel 0:
1. Pixel 0 <= 4*Int(858/4)
2. Required pixel 0 < 214 therefore quadrant = 0, [PG[10:9] = 00]
3. PG[10:0] = 511 - 214 + (0+[0*214]) = 297

Pixel 56:
1. Pixel 56 <= 4*Int(858/4)
2. Required pixel 56 < 214 therefore quadrant = 0 [PG[10:9] = 00]
3. PG[10:0] = 511 - 214 + (56-[0*214]) = 353

Pixel 250:
1. Pixel 250 <= 4*Int(858/4)
2. Required pixel 250 > 214 therefore quadrant =/= 0
3. Required pixel 250 < 428 therefore quadrant = 1, [PG[10:9] = 01]
4. PG[10:0] = 1023 - 214 + (250-[1*214]) = 845

Pixel 800:
1. Pixel 800 <= 4*Int(858/4)
2. Required pixel 800 > 214 therefore quadrant =/= 0
3. Required pixel 800 > 428 therefore quadrant =/= 1
4. Required pixel 800 > 642 therefore quadrant =/= 2
5. Required pixel 800 < 858 therefore quadrant = 3, [PG[10:9] = 11]
6. PG[10:0]= 2047 - 214 + (800-[3*214]) = 1991

Pixel 856:
1. Pixel <= 4*Int(858/4)
2. Required pixel 856 > 214 therefore quadrant =/= 0
3. Required pixel 856 > 428 therefore quadrant =/= 1
4. Required pixel 856 > 642 therefore quadrant =/= 2
5. Required pixel 856 < 858 therefore quadrant = 3, [PG[10:9] = 11]
6. PG[10:>0] = 2047 - 214 + (856-[3*214]) = 2047

Pixel 857:
1. Pixel 857 > 4*Int(858/4)
2. Therefore quadrant = 3, [PG[10:9] = 11]
3. PG[10:0] = 1536 + (857-[4*214]) = 1537

Composite Line Grab

The composite line grab is only available in the 3 line comb based decoders (TMC22053 and TMC22153), and allows the user to grab any line from the 4 field sequence in NTSC or 8 field sequence in PAL when LGEN is set HIGH. When the LGEN register bit is set HIGH the decoder automatically switches to operate as a "simple" bandsplit decoder. The SET pin can also be used to produce the line grab pulse if SET_{2-0} = 110 and LGEXT is set HIGH.

Once the line grab has been activated the subcarrier oscillator is frozen with the SEED and phase from the beginning of the line, and the composite video in the 1H line store is frozen by disabling the write signals in LSTORE1. The read cycle for the frozen line store is still clocked by PCK. The subcarrier DDS and the internal read only registers will be updated once per clock period as normal, but will reload the DRS SEED and PHASE values at the beginning of each line. The G/Y, B/U, and R/V outputs will remain active, and the $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$ signals will remained locked to the input or flywheel if the input has been removed.

The pixel grab function can be used in conjunction with the frozen line to examine individual pixels inside the decoder.

Parallel Microprocessor Interface

The parallel microprocessor interface, active when $\overline{\text{SER}}$ is HIGH, employs a 12-line interface, with an 8-bit data bus and one address bit: two addresses are required for device programming and pointer-register management. Address bit 0 selects between reading/writing the register addresses and reading/writing register data. When writing, the address is presented along with a LOW on the $\overline{\text{R/W}}$ pin during the falling edge of $\overline{\text{CS}}$ Eight bits of data are presented on D_{7-0} during the subsequent rising edge of $\overline{\text{CS}}$. One additional falling edge of $\overline{\text{CS}}$ is needed to move input data to its assigned working registers.

In read mode, the address is accompanied by a HIGH on the $\overline{\text{R/W}}$ pin during a falling edge of $\overline{\text{CS}}$. The data output pins go to a low-impedance state t_{DOZ} after $\overline{\text{CS}}$ falls. Valid data are present on D_{7-0} t_{DOM} after the falling edge of $\overline{\text{CS}}$. Because this port operates asynchronously with the pixel timing, there is an uncertainty in this data valid output delay of one PXCK period. This uncertainty does not apply to t_{DOZ}.

Writing data to specific control registers of the TMC22x5y requires that the 8-bit address of the control register of interest be written. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 3Fh.

Table 24. Parallel Port Control

A_{1-0}	$\overline{\text{R/W}}$	Action
00	0	Load D_{7-0} into Control Register pointer (block 00)
00	1	Read Control Register pointer on D_{7-0}
01	0	Load D_{7-0} into addressed XLUT Location pointer (block 01)
01	1	Read addressed XLUT Location pointer on D_{7-0}.
10	0	Write D_{7-0} to addressed Control Register
10	1	Read addressed Control Register on D_{7-0}
11	0	Write D_{7-0} to addressed XLUT Location
11	1	Read addressed XLUT Location on D_{7-0}

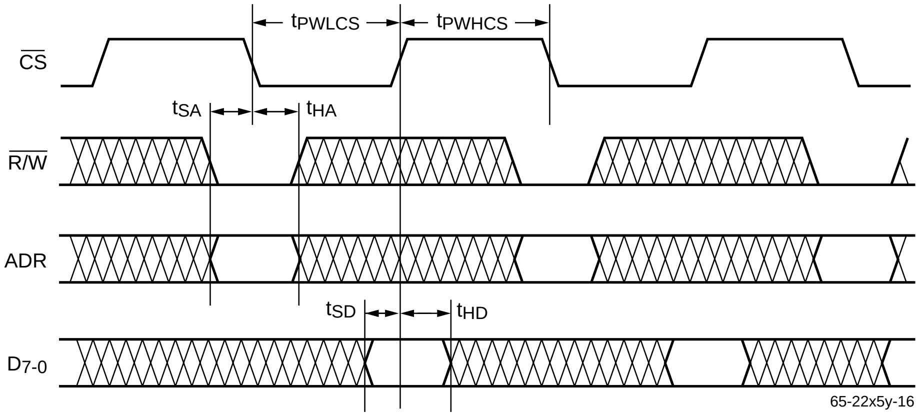


Figure 33. Microprocessor Parallel Port – Write Timing

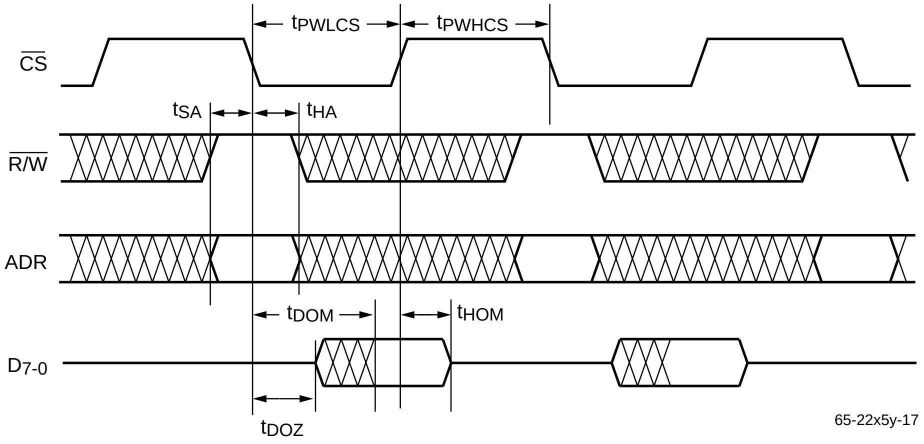


Figure 34. Microprocessor Parallel Port – Read Timing

Serial Control Port (R-Bus)

In addition to the 12-wire parallel port, a 2-wire serial control interface is provided, and active when $\overline{\text{SER}}$ is LOW. Either port alone can control the entire chip. Up to eight TMC22x5y devices may be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The Decoder acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

- Start signal
- Slave address byte
- Block Pointer
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are HIGH) communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a seven bit slave address (the first seven bits) and a single $\overline{\text{R/W}}$ bit (the eighth bit). The $\overline{\text{R/W}}$ bit indicates the direction of data transfer, read from or write to the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA_{2-0} input pins in Table 20), the TMC22x5y acknowledges by bringing SDA LOW on the 9th SCL pulse. If the addresses do not match, the TMC22x5y does not acknowledge.

Table 25. Serial Port Addresses

bit 7 A_6 (MSB)	bit 6 A_5	bit 5 A_4	bit 4 A_3	bit 3 A_2 (SA_2)	bit 2 A_1 (SA_1)	bit 1 A_0 (SA_0)
1	0	1	1	0	0	0
1	0	1	1	0	0	1
1	0	1	1	0	1	0
1	0	1	1	0	1	1
1	0	1	1	1	0	0
1	0	1	1	1	0	1
1	0	1	1	1	1	0
1	0	1	1	1	1	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the TMC22x5y does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the TMC22x5y during a read sequence, the Decoder interprets this as “end of data.” The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the TMC22x5y requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 3Fh. Any base address higher than 3Fh will not produce an ACKnowledge signal.

Data are read from the control registers of the TMC22x5y in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W\ bit of the slave address byte LOW to set up a sequential read operation.

Reading (the $\overline{\text{R/W}}$ bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the TMC22x5y, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to one control register

- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = LOW)
- Block Pointer (00)
- Base Address byte
- Data byte to base address
- Stop signal

Write to four consecutive XLUT locations

- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = LOW)
- Block Pointer (01)
- Base Address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one XLUT location

- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = LOW)
- Block Pointer (01)
- Base Address byte
- Stop signal

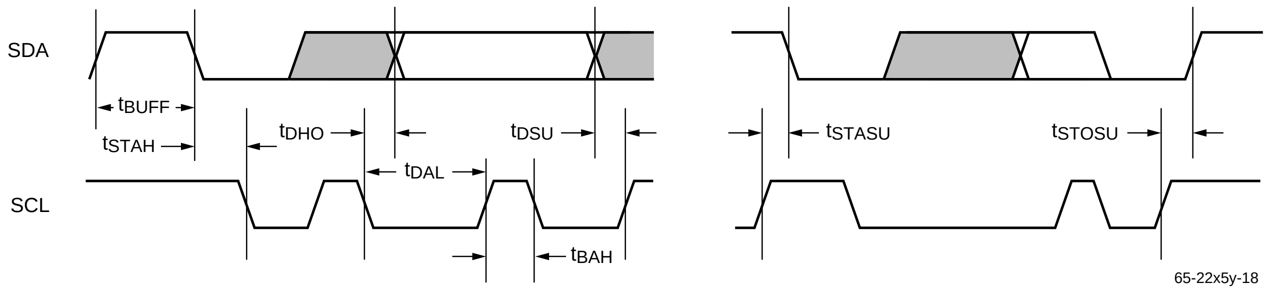


Figure 35. Serial Port Read/Write Timing

- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = HIGH)
- Data byte from base address
- Stop signal

Read from four consecutive control registers

- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = LOW)
- Block Pointer (00)
- Base Address byte
- Stop signal
- Start signal
- Slave Address byte ($\overline{\text{R/W}}$ bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

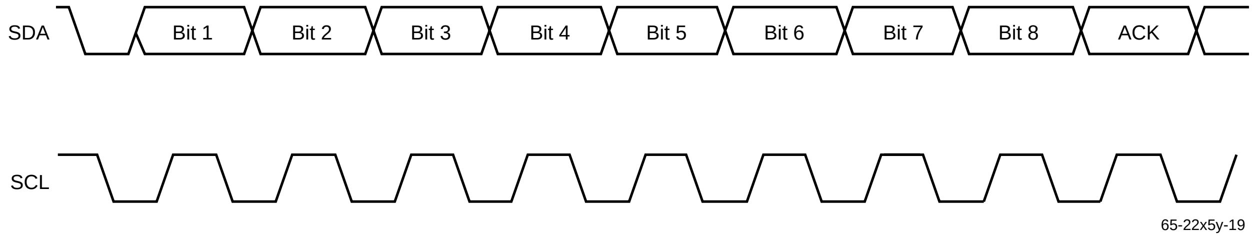


Figure 36. Serial Interface – Typical Byte Transfer

Equivalent Circuits and Threshold Levels

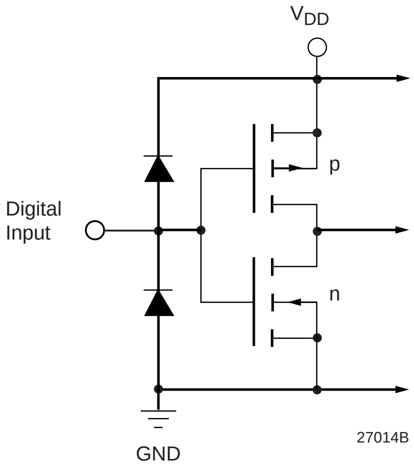


Figure 37. Equivalent Digital Input Circuit

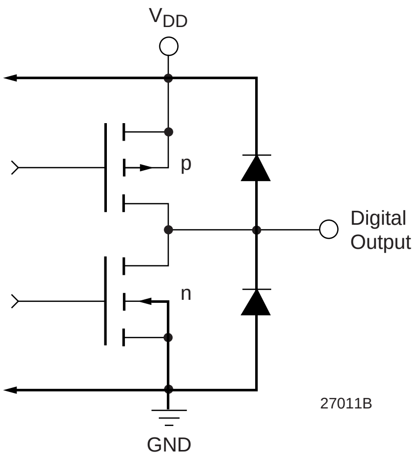


Figure 38. Equivalent Digital Output

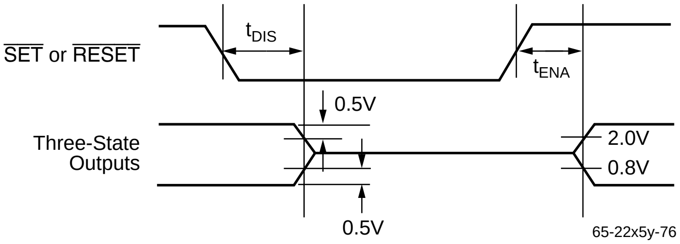


Figure 39. Threshold Levels for Three-state

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Unit
Power Supply voltage	-0.5	+7.0	V
Digital Inputs			
Applied Voltage	-0.5	V_{DD}+0.5	V
Forced current [3, 4]	-20.0	+20.0	mA
Digital Outputs			
Applied voltage [2]	-0.5	V_{DD}+0.5	V
Forced current [3, 4]	-3.0	+6.0	mA
Short circuit duration (single output in HIGH state to ground)		1 second	
Analog Output Short circuit duration (all outputs to ground)		infinite	
Temperature			
Operating, ambient	-20	110	°C
junction		140	°C
Lead, soldering (10 seconds)		300	°C
Vapor Phase soldering (1 minute)		220	°C
Storage		150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Preliminary Information

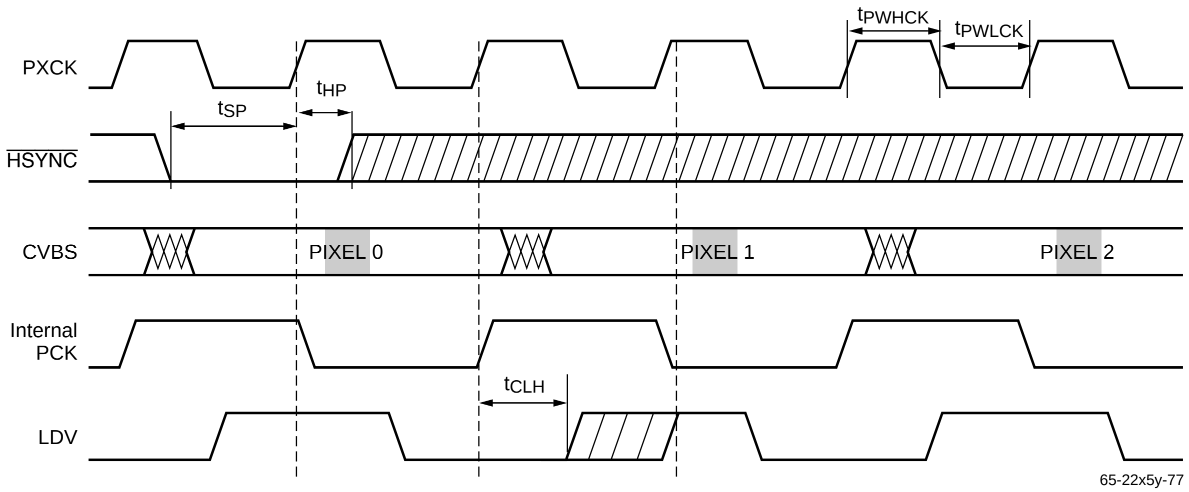


Figure 40. Input Timing Parameters

Operating Conditions

Parameter		Min.	Nom.	Max.	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Compatible Inputs	2.0		V_{DD}	V
	Serial Port (SDA and SCL)	0.7*V_{DD}			V
V_{IL}	Input Voltage, Logic LOW				
	TTL Compatible Inputs	GND		0.8	V
	Serial Port (SDA and SCL)	GND		0.3*V_{DD}	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C
Pixel Interface (input)					
f_{CLK}	Pixel Rate (CKSEL = 0)	10		18	MHz
	Master Clock Rate = 2X pixel rate (CKSEL = 1)[1]	20		36	MHz
t_{PWHCK}	CLOCK pulse width, HIGH	8			ns
t_{PWLCK}	CLOCK pulse width, LOW	13			ns
t_{SP}	Pixel Data Input Setup Time	8			ns
t_{HP}	Pixel Data Input Hold Time	2			ns
t_{SP}	$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and BUFFER setup time	5			ns
t_{HP}	$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and BUFFER hold time	6			ns

Notes:

1. Tested at f_{CLK} = 30MHz

To aid in the understanding of the timing relationship between the PXCK and LDV clock, when the LDV signal is used as the TMC22x5y output clock, the following block diagram of the TMC22x5y output stage is provided.

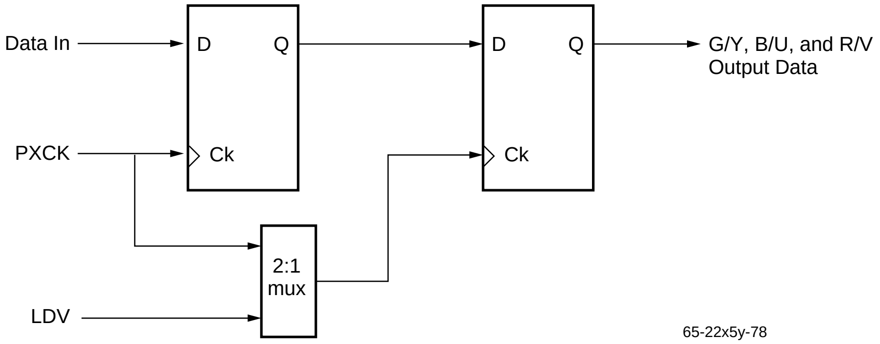


Figure 41. Functional Block Diagram of the TMC22x5y G/Y, B/U, and R/V Output Stage

Operating Conditions (continued)

Parameter		Min.	Nom.	Max.	Units
Pixel Interface (output)					
t_{POD}	CLOCK to $\overline{\text{DHSYNC}}$ and $\overline{\text{DVYSNC}}$, AVOUT, and FID$_{[2:0]}$ Propagation Time	4	15	18	ns
t_{POD}	CLOCK to data, Propagation Time	4	15	18	ns
t_{POD}	Int. or Ext. LDV to data, Propagation Time	4	15	18	ns
t_{HOD}	Clock to $\overline{\text{DHSYNC}}$ and $\overline{\text{DVSYNC}}$, AVOUT, and FID$_{[2:0]}$ Hold Time	2.5			ns
t_{HOD}	Clock to Data, Hold Time	2.5			ns
t_{HOD}	Int. or Ext. LDV to Data, Hold Time	2.5			ns
t_{ENA}	Enable to Low Z on Output Data		23	30	ns
t_{DIS}	Disable to High Z on Output Data		23	30	ns
t_{CLH}	CLOCK to LDV (i/p) signal HIGH	9		0	ns
t_{CLH}	CLOCK to LDV (o/p) signal HIGH		10	14	ns

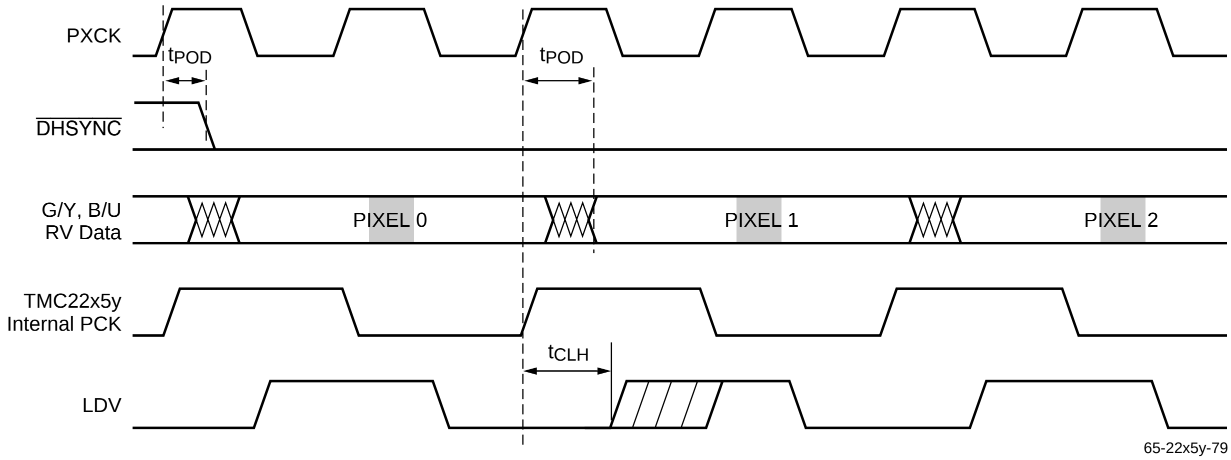


Figure 42. Output Timing Parameters

Preliminary Information

Preliminary Information

Operating Conditions (continued)

Parameter		Min.	Nom.	Max.	Units
Parallel Microprocessor Interface					
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW	2			Pixels
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH	3			Pixels
t_{SA}	Address Setup Time	8			ns
t_{HA}	Address Hold Time	2			ns
t_{SD}	Data Setup Time (write)	8			ns
t_{HD}	Data Hold Time (write)	2			ns
Serial Microprocessor Interface					
t_{DAL}	SCL Pulse Width , LOW	1.0			µs
t_{DAH}	SCL Pulse Width, HIGH	0.48			µs
t_{STAH}	Hold Time for START or Repeated START	0.48			µs
t_{STASU}	Setup Time for START or Repeated START	0.48			µs
t_{STOSU}	Setup time for STOP	0.48			µs
t_{BUFF}	Bus Free Time Betweeen a STOP and a START condition	1.0			µs
t_{DSU}	Data Setup Time	80			ns

Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current[1]	V_{DD} = Max, f_{PXCK} = 27MHz		225	275	mA
I_{DDQ}	Power Supply Current, Disabled	V_{DD} = Max			50	mA
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V			±10	µA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	G/Y_{9-0}, etc[2]., I_{OH} = MAX	2.4			V
V_{OL}	Output Voltage, LOW	G/Y_{9-0}, etc[2]., I_{OL} = MAX			0.4	V
		SDA, I_{OL} = 3mA			0.4	V
		SDA, I_{OL} = 6mA			0.6	V
C_I	Digital Input Capacitance			4	10	pF
C_O	Digital Output Capacitance			10		pF

Notes:

1. Typical I_{DD} with V_{DD} = NOM and T_A = NOM, Maximum I_{DD} with V_{DD} = 5.25V and T_A = 70°C
2. G/$Y_{[9:0]}$, B/$Y_{[9:0]}$, R/$V_{[9:0]}$, $\overline{DVSYNC}$, $\overline{DHSYNC}$, LDV, AVOUT, $FID_{[2:0]}$

Switching Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		9			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		10			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			30	40	ns

Note:

Timing reference points are at the 50% level, digital output load <40pF.

System Performance Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
RES	Video Processing Resolution	TMC2205x		8		bits
		TMC2215x		10		bits

Preliminary Information

Programming Examples

Standard: NTSC-M

Mode: Line-Locked

Input Format: 13.5 Composite

Output Format: RGB (0-1023) Sync on Green

Decoder: Adaptive 3-Line Chroma Comb Filter

Register Map:

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0	D8	01	00	A1	20	28	00	10	40	00	12	00	00	04	24	09
1	5A	56	2E	D2	23	00	00	2C	1B	90	13	49	F0	01	00	00
2	40	F8	E0	43	00	00	07	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Standard: NTSC

Mode: Line-Locked

Input Format: NTSC Composite

Output Format: D1 Component

Decoder: 3 Line Adaptive Chroma Comb

Register Map:

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0	C0	01	00	A1	20	28	00	10	40	00	34	74	80	04	64	08
1	5A	56	2E	D2	23	72	00	00	95	0E	51	49	40	00	00	00
2	40	F8	E0	43	24	25	07	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Programming Examples (continued)

Standard: NTSC

Mode: Line-Locked

Input Format: 13.5 MHz Composite Video

Output Format: YUV

Decoder: Adaptive 3-Line Comb

Register Map:

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0	D8	01	00	A1	20	28	00	10	40	00	34	00	80	04	64	08
1	5A	56	2E	D2	23	3C	00	2C	1B	90	13	49	F0	01	00	00
2	40	F8	E0	43	24	25	07	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Standard: PAL

Mode: Line-Locked

Input Format: Composite

Output Format: YUV

Decoder: Adaptive 3-Line Comb

Register Map:

	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
0	DB	01	00	24	08	00	24	15	40	08	36	00	C0	04	54	09
1	60	53	32	CE	23	01	00	00	00	3E	03	49	00	05	00	00
2	90	15	13	54	24	25	07	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Programming Examples (continued)

Standard: PAL

Mode: Line-Locked

Input Format: PAL-YC

Output Format: Y, Cb, Cr (D1 Out)

Decoder:

Register Map: No Comb

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	D3	07	00	00	20	00	00	0C	40	08	24	60	03	00	0B	0A
1	60	53	44	D2	23	00	00	00	88	BF	3C	49	40	00	00	00
2	90	15	13	54	00	00	00	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Standard: NTSC-M

Mode: D1 Mode

Input Format: D1, C_BYC_R [Y] multiplexed data w/embedded TRS words

Output Format: D1 Output

Decoder: 2 Line Chroma comb of C_BC_R data

Register Map:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	1F	37	E3	20	00	00	0C	40	40	34	60	09	04	F8	02
1	5A	47	35	D2	23	00	0A	00	00	00	00	49	40	00	00	00
2	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Programming Examples (continued)

Standard: NTSC-M

Mode: D1 Mode

Input Format: D1, C_BYC_R [Y] Multiplexed Data w/TRS

Output Format: YC_BC_R, Output DHSync + DVSync

Decoder: Simple Transcoder

Register Map:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	1F	37	E3	20	00	00	0C	40	40	34	00	09	04	0A	02
1	5A	47	35	D2	23	00	0A	00	00	00	00	49	40	00	00	00
2	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Standard: NTSC-M

Mode: D1 Mode

Input Format: YC_BC_R

Output Format: D1, C_BYC_R [Y] Multiplexed Data with TRS

Decoder: Simple Transcoder

Register Map:

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	C0	0F	07	A3	20	00	00	0C	40	00	34	60	09	04	0A	02
1	5A	47	35	D2	23	00	00	00	00	00	00	49	40	00	00	00
2	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
3	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Programming Worksheet

Standard:

Mode:

Input Format:

Output Format:

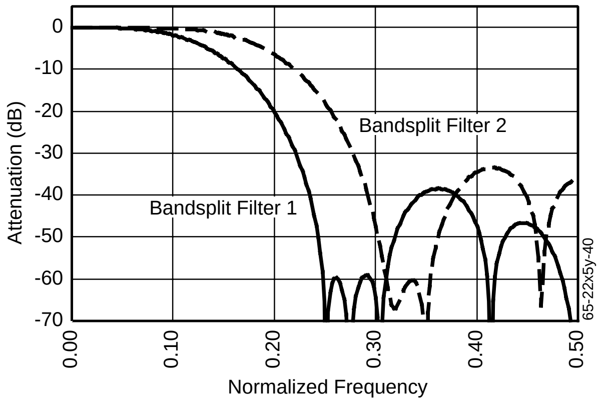
Decoder:

Register Map:

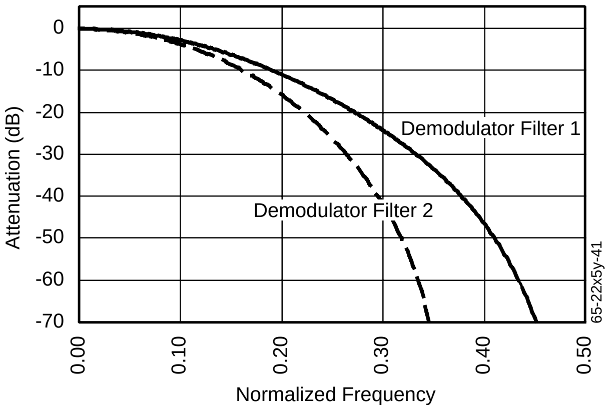
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2								xx	xx	xx	xx	xx	xx	xx	xx	xx

The DRS appears on the output at the rate.

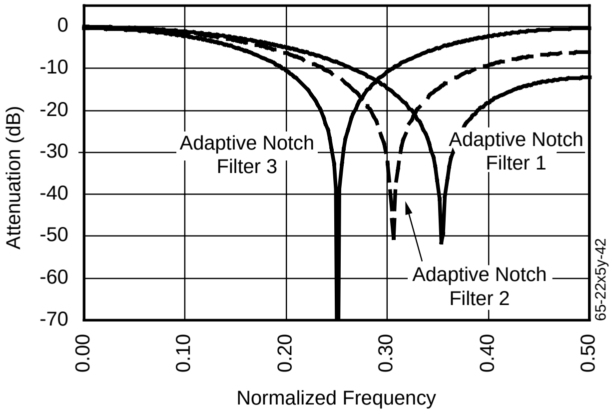
Bandsplit Filter



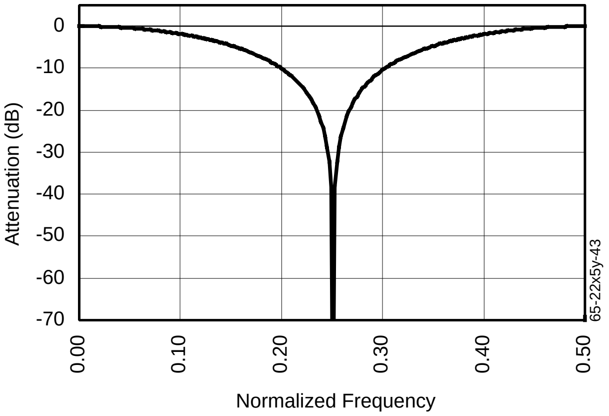
Demodulation Filter



Adaptive Notch Filter



Non-Adaptive Notch Filter



Related Products

- TMC22071 Genlocking Video Digitizer
- TMC22x9x Digital Video Encoders
- TMC2081 Digital Video Mixer
- TMC3003 Triple 10-bit D/A Converter

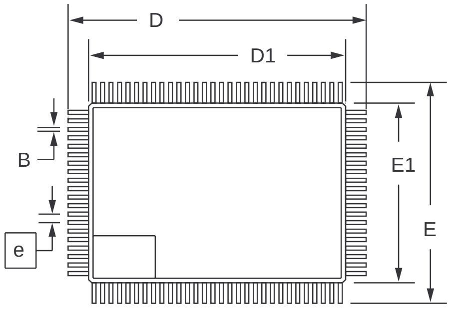
Notes:

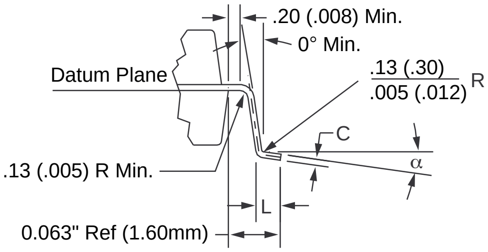
Mechanical Dimensions – 100 Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.134	—	3.40	
A1	.010	—	.25	—	
A2	.100	.120	2.55	3.05	
B	.009	.015	.23	.38	3, 5
C	.005	.009	.13	.23	5
D	.904	.923	22.95	23.45	
D1	.783	.791	19.90	20.10	
E	.667	.687	16.95	17.45	
E1	.547	.555	13.90	14.10	
e	.0256 BSC		.65 BSC		
L	.025	.037	.65	.95	4
N	100		100		
ND	30		30		
NE	20		20		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

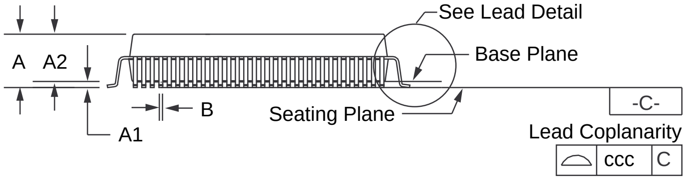
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail



Preliminary Information

Ordering Information

Product Number	Temperature Range	Decoding	Resolution	Package	Package Marking
TMC22051KHC	0°C to 70°C	Simple	8 bit	100-Lead MQFP	22051KHC
TMC22052KHC	0°C to 70°C	2-Line Comb	8 bit	100-Lead MQFP	22052KHC
TMC22053KHC	0°C to 70°C	3-Line Comb	8 bit	100-Lead MQFP	22053KHC
TMC22151KHC	0°C to 70°C	Simple	10 bit	100-Lead MQFP	22151KHC
TMC22152KHC	0°C to 70°C	2-Line Comb	10 bit	100-Lead MQFP	22152KHC
TMC22153KHC	0°C to 70°C	3-Line Comb	10 bit	100-Lead MQFP	22153KHC

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